

Contents

1	Introduction	1
1.1	Exercises	4
2	Silicon Wafer Production	5
2.1	Silicon as Basic Material	5
2.2	Production and Purification of the Raw Material	7
2.2.1	Production of Technical Silicon	7
2.2.2	Chemical Purification of the Technical Grade Silicon	8
2.2.3	Zone Purification	9
2.3	Production of Single Crystals	10
2.3.1	The Crystal Structure	10
2.3.2	Crystal Pulling Method According to Czochralski	12
2.3.3	Crucible-Free Zone Pulling	14
2.3.4	Crystal Defects	15
2.4	Crystal Processing	16
2.4.1	Dicing	16
2.4.2	Surface Treatment	17
2.5	Tasks for Slice Production	19
	References	20
3	Oxidation of Silicon	21
3.1	Thermal Oxidation of Silicon	22
3.1.1	Dry Oxidation	23
3.1.2	Wet Oxidation	23
3.1.3	H ₂ O ₂ Combustion	24
3.2	Modelling of the Oxidation	25
3.3	The SiO ₂ /Silicon Interface	27
3.4	Segregation	28

3.5	Deposition Processes for Silicon Dioxide	30
3.5.1	Silane Pyrolysis	30
3.5.2	TEOS Oxide Deposition	31
3.6	Tasks for the Oxidation of Silicon	31
	References	32
4	Lithography	33
4.1	Mask Technique	34
4.1.1	Pattern Generator and Step-And-Repeat Exposure	35
4.1.2	Direct Writing of the Mask with the Electron Beam	35
4.1.3	Mask Techniques for Highest Resolutions.	36
4.2	Resist Coating	37
4.2.1	Structure of the Photoresists	37
4.2.2	Deposition of the Photoresist Layer.	38
4.3	Exposure Procedure	40
4.3.1	Optical Lithography (Photolithography)	40
4.3.2	Electron Beam Lithography	47
4.3.3	X-ray Lithography	50
4.3.4	Further Procedures for Structuring	51
4.4	Resist Processing	54
4.4.1	Developing and Curing the Photoresist	54
4.4.2	Line Width Control	55
4.4.3	Removing the Resist Mask	56
4.5	Lithography Tasks	58
	References	58
5	Etching Technology	59
5.1	Wet Chemical Etching	60
5.1.1	Dip Etching	61
5.1.2	Spray Etching	61
5.1.3	Etching Solutions for Wet-Chemical Structuring	61
5.2	Dry Etching	64
5.2.1	Plasma Etching (PE)	65
5.2.2	Reactive Ion Etching (RIE)	67
5.2.3	Ion Beam Etching	73
5.2.4	Dry Etching Process for High Etch Rates	73
5.2.5	Atomic Layer Etching (ALE)	75
5.3	Endpoint Detection	76
5.3.1	Visual Control	76
5.3.2	Ellipsometry	77
5.3.3	Optical Spectroscopy	77
5.3.4	Interferometry	78
5.3.5	Mass Spectrometry	78

5.4	Etching Tasks	78
	References	79
6	Doping Techniques	81
6.1	Alloying	82
6.2	Diffusion	84
6.2.1	Fick's Laws	85
6.2.2	Diffusion Process	88
6.2.3	Implementation of the Diffusion Process	90
6.2.4	Limitations of the Diffusion Technique	91
6.3	Ion Implantation	92
6.3.1	Range of Implanted Ions	92
6.3.2	Channeling	93
6.3.3	Activation of the Dopants	94
6.3.4	Technical Design of an Ion Implanter	97
6.3.5	Characteristics of Implantation	100
6.4	Tasks for the Doping Techniques	101
	References	102
7	Deposition Process	103
7.1	Chemical Deposition Processes	103
7.1.1	The Silicon Gas-Phase Epitaxy	103
7.1.2	The CVD Process for Layer Deposition	106
7.1.3	Atomic Layer Deposition (ALD)	112
7.2	Physical Deposition Processes	114
7.2.1	Molecular Beam Epitaxy (MBE)	114
7.2.2	Evaporation	115
7.2.3	Sputtering	117
7.3	Tasks for the Separation Techniques	120
	References	121
8	Metallization and Contacts	123
8.1	The Metal–Semiconductor Contact	124
8.2	Multi-Layer Wiring	127
8.2.1	Planarisation Techniques	128
8.2.2	Filling Contact Openings and Vias	132
8.3	Reliability of Aluminium Metallization	133
8.4	Copper Metallization	134
8.5	Metallization Tasks	137
	References	138

9	Wafer Cleaning	139
9.1	Impurities and Their Effects.	140
9.1.1	Microscopic Impurities	141
9.1.2	Molecular Impurities	141
9.1.3	Alkaline and Atomic Impurities.	142
9.2	Cleaning Techniques	143
9.3	Etching Solutions for Substrate Cleaning	144
9.4	Example of a Cleaning Sequence	145
9.5	Tasks for Substrate Cleaning	146
	Reference	147
10	MOS Technologies for Circuit Integration	149
10.1	Single-Channel MOS Techniques	150
10.1.1	The PMOS Aluminium Gate Process	150
10.1.2	The n-Channel Aluminium Gate MOS Technique.	152
10.1.3	The n-Channel Silicon Gate MOS Technology	155
10.2	The n-Well Silicon Gate CMOS Process	158
10.2.1	Circuit Elements of the CMOS Technology	164
10.2.2	Latchup Effect	168
10.3	Test and Parameter Acquisition	171
10.4	Tasks for the MOS Technique	172
	References	174
11	Developments for High-Density Integrated Circuits	175
11.1	Local Oxidation of Silicon (LOCOS)	175
11.1.1	The Simple Local Oxidation of Silicon	176
11.1.2	SPOT Technique for Local Oxidation	178
11.1.3	The SILO Technique	179
11.1.4	Poly-Buffered LOCOS	180
11.1.5	The SWAMI LOCOS Technique	181
11.1.6	Trench Isolation	184
11.2	Advanced MOS Transistors for High-Density Integrated Circuits	185
11.2.1	Breakdown Mechanisms in MOS Transistors	187
11.2.2	The Spacer Technique for Doping Optimisation	189
11.2.3	Self-Aligned Contacts	195
11.3	SOI Techniques	197
11.3.1	SOI Substrates	197
11.3.2	Process Control in SOI Technology	204

11.4	Transistors with Nanometer Dimensions	205
11.4.1	Requirements for Further Scaling	205
11.4.2	Analysis of Nanometer-Scale n-type Field-Effect Transistors	208
11.4.3	The FINFET in SOI Technology	209
11.4.4	FINFET in the Standard Silicon Substrate.	210
11.5	Tasks for High-Density Integrated Circuits	211
	References.	212
12	Bipolar Technology	215
12.1	The Standard Buried Collector Technique.	216
12.2	Advanced SBC Technique	218
12.3	Bipolar Process with Self-Aligned Emitter	219
12.4	BiCMOS Techniques	222
12.5	Bipolar Technology Tasks	224
	References.	224
13	Packaging of Integrated Circuits.	225
13.1	Preparing the Wafers for Packaging.	226
13.1.1	Reducing the Wafer Thickness.	226
13.1.2	Reverse Side Metallization	227
13.1.3	Separation of the Chips	227
13.2	Assembly	229
13.2.1	Substrates/System Carriers	229
13.2.2	Die Bonding.	231
13.3	Electrical Contacts	233
13.3.1	Single Wire Bonding	233
13.3.2	Simultaneous Contacting	238
13.4	Finishing the Packages.	243
13.5	Chip Assembly Tasks.	244
	References.	244
	Annexes	245