

Table of Contents

Invited Program

Embedded Systems as Datacenters (Keynote)	1
<i>Bob Iannucci</i>	
Larrabee: A Many-Core Intel Architecture for Visual Computing (Keynote)	2
<i>Roger Espasa</i>	

Architectural Support for Concurrency

Remote Store Programming: A Memory Model for Embedded Multicore	3
<i>Henry Hoffmann, David Wentzlaff, and Anant Agarwal</i>	
Low-Overhead, High-Speed Multi-core Barrier Synchronization	18
<i>John Sartori and Rakesh Kumar</i>	
Improving Performance by Reducing Aborts in Hardware Transactional Memory	35
<i>Mohammad Ansari, Behram Khan, Mikel Luján, Christos Kotselidis, Chris Kirkham, and Ian Watson</i>	
Energy and Throughput Efficient Transactional Memory for Embedded Multicore Systems	50
<i>Cesare Ferri, Samantha Wood, Tali Moreshet, Iris Bahar, and Maurice Herlihy</i>	

Compilation and Runtime Systems

Split Register Allocation: Linear Complexity Without the Performance Penalty	66
<i>Boubacar Diouf, Albert Cohen, Fabrice Rastello, and John Cavazos</i>	
Trace-Based Data Layout Optimizations for Multi-core Processors	81
<i>Olga Golovanevsky, Alon Dayan, Ayal Zaks, and David Edelsohn</i>	
Buffer Sizing for Self-timed Stream Programs on Heterogeneous Distributed Memory Multiprocessors	96
<i>Paul M. Carpenter, Alex Ramirez, and Eduard Ayguadé</i>	
Automatically Tuning Sparse Matrix-Vector Multiplication for GPU Architectures	111
<i>Alexander Monakov, Anton Lokhmotov, and Arutyun Avetisyan</i>	

Reconfigurable and Customized Architectures

Virtual Ways: Efficient Coherence for Architecturally Visible Storage in Automatic Instruction Set Extensions	126
<i>Theo Kluter, Samuel Burri, Philip Brisk, Edoardo Charbon, and Paolo Ienne</i>	
Accelerating XML Query Matching through Custom Stack Generation on FPGAs	141
<i>Roger Moussalli, Mariam Salloum, Walid Najjar, and Vassilis Tsotras</i>	
An Application-Aware Load Balancing Strategy for Network Processors	156
<i>Rainer Ohlendorf, Michael Meitinger, Thomas Wild, and Andreas Herkersdorf</i>	
Memory-Aware Application Mapping on Coarse-Grained Reconfigurable Arrays	171
<i>Yongjoo Kim, Jongeun Lee, Aviral Shrivastava, Jonghee Yoon, and Yunheung Paek</i>	

Multicore Efficiency, Reliability, and Power

Maestro: Orchestrating Lifetime Reliability in Chip Multiprocessors	186
<i>Shuguang Feng, Shantanu Gupta, Amin Ansari, and Scott Mahlke</i>	
Combining Locality Analysis with Online Proactive Job Co-scheduling in Chip Multiprocessors	201
<i>Yunlian Jiang, Kai Tian, and Xipeng Shen</i>	
RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor	216
<i>Houman Homayoun, Aseem Gupta, Alex Veidenbaum, Avesta Sasan (M.A. Makhzan), Fadi Kurdahi, and Nikil Dutt</i>	
Performance and Power Aware CMP Thread Allocation Modeling	232
<i>Yaniv Ben-Itzhak, Israel Cidon, and Avinoam Kolodny</i>	

Memory Organization and Optimization

Multi-level Hardware Prefetching Using Low Complexity Delta Correlating Prediction Tables with Partial Matching	247
<i>Marius Grannaes, Magnus Jahre, and Lasse Natvig</i>	
Scalable Shared-Cache Management by Containing Thrashing Workloads	262
<i>Yuejian Xie and Gabriel H. Loh</i>	

SRP: Symbiotic Resource Partitioning of the Memory Hierarchy in CMPs	277
<i>Shekhar Srikantaiah and Mahmut Kandemir</i>	
DIEF: An Accurate Interference Feedback Mechanism for Chip Multiprocessor Memory Systems	292
<i>Magnus Jahre, Marius Grannaes, and Lasse Natvig</i>	
 Programming and Analysis of Accelerators	
<i>Tagged Procedure Calls (TPC): Efficient Runtime Support for Task-Based Parallelism on the Cell Processor</i>	307
<i>George Tzenakis, Konstantinos Kapelonis, Michail Alvanos, Konstantinos Koukos, Dimitrios S. Nikolopoulos, and Angelos Bilas</i>	
Analysis of Task Offloading for Accelerators	322
<i>Roger Ferrer, Vicenç Beltran, Marc González, Xavier Martorell, and Eduard Ayguadé</i>	
Offload - Automating Code Migration to Heterogeneous Multicore Systems	337
<i>Pete Cooper, Uwe Dolinsky, Alastair F. Donaldson, Andrew Richards, Colin Riley, and George Russell</i>	
Computer Generation of Efficient Software Viterbi Decoders	353
<i>Frédéric de Mesmay, Srinivas Chellappa, Franz Franchetti, and Markus Püschel</i>	
Author Index	369