

Contents

1	Advanced Electronic Packaging	1
1.1	Introduction	1
1.2	Adhesively Bonded Multilayer Structure	5
1.3	Interfacial Peeling-off	6
1.3.1	Needle Ejecting for Thin Chips	6
1.3.2	Conformal Peeling for Large-Area Devices	8
1.3.3	LLO for Large-Area Flexible Electronics	9
1.4	Vacuum-Based Chip Picking-up	12
1.5	Vacuum-Based Chip Placing-on	13
1.6	Competing Fracture	16
1.6.1	Competing Fracture Behavior	16
1.6.2	Fracture Strength and Adhesive Fracture Energy	16
	References	17
2	Interfacial Modeling of Flexible Multilayer Structures	29
2.1	Introduction	29
2.2	Modeling of Chip-on-Substrate Structure	29
2.2.1	Mechanical Model	29
2.2.2	Analytical Evaluation on ERR of Interfacial Peeling	31
2.2.3	Virtual Crack Closure Technique (VCCT)	33
2.2.4	Numerical Model	34
2.3	Modeling of Chip-Adhesive-Substrate Adhesively Bonded Joints	34
2.3.1	Adhesive Model on Overlapped Joints	34
2.3.2	Equilibrium Equations	36
2.3.3	Establishment of Differential Equation Set	38
2.3.4	Solutions for Internal Forces and Displacements	40
2.3.5	Relationships Among Integration Constants	44
2.3.6	Theoretical Calculation of ERR of Interfacial Peeling	46

2.4	Summary	46
	References	47
3	Measurement of Fracture Strength of Ultra-thin Silicon Chip and Adhesive Fracture Energy	49
3.1	Introduction	49
3.2	Fracture Strength of Ultra-thin Silicon Chip	50
3.2.1	Experimental Procedure	50
3.2.2	Nonlinear Mechanical Characterization in Bending Test	51
3.2.3	Estimation of Fracture Strength	58
3.3	Estimation of Adhesive Fracture Energy of Adhesive Tape	62
3.3.1	Theoretical Foundation	62
3.3.2	Experimental Procedure	64
3.3.3	Estimation of Adhesive Fracture Energy	64
3.3.4	Angle Dependence of Peel Force	65
3.3.5	Rate Dependence of Adhesive Fracture Energy	67
3.4	Summary	69
	References	70
4	Tension-Assisted Peeling	73
4.1	Introduction	73
4.2	Theoretical Determination of Integration Constants	73
4.2.1	Stiffened Plate Joint Under Axial Tension and Bending Moment	74
4.2.2	Single-Strap Joint Under Tension	76
4.2.3	Single-Lap Joint Under Tension	79
4.3	Modeling of Adhesively Bonded Chip Array	82
4.3.1	Mechanical Model Description	82
4.3.2	Boundary and Continuity Conditions	84
4.3.3	Solution for Internal Forces and Displacements	85
4.3.4	Determination of Integration Constants	86
4.4	Adhesive Stresses for Adhesively Bonded Joints	87
4.4.1	Analysis of Balanced Adhesively Bonded Joints	87
4.4.2	Analysis of Unbalanced Adhesively Bonded Joints	90
4.4.3	Discussion of Results	92
4.5	Peeling Behavior for Chip Array on Stretched Substrate	93
4.5.1	Adhesive Stresses	93
4.5.2	Effect of Geometric Dimensions	95
4.5.3	Effect of Material Properties	98
4.5.4	Process Optimization	100
4.6	Summary	101
	References	102

5	Single-needle Peeling	105
5.1	Introduction	105
5.2	A Case for Chip-on-Substrate Structure	107
5.2.1	Effect of Crack Length	108
5.2.2	Effect of Geometric Dimensions	108
5.2.3	Effect of Elastic Mismatch	110
5.3	A Case for Chip-Adhesive-Substrate Structure	111
5.3.1	Geometric Model Description	111
5.3.2	Theoretical Calculation of ERR	115
5.3.3	Effect of Crack Length	116
5.3.4	Effect of Geometric Dimensions	117
5.3.5	Effect of Material Properties	118
5.3.6	Analysis on Tunability of Peeling Mode	119
5.4	Analysis of Fracture Mode Based on Competing Index	121
5.4.1	Typical Fracture Modes	121
5.4.2	Competing Fracture Model	123
5.4.3	Basic Fracture Parameters	124
5.4.4	Effect of Geometric Dimensions	125
5.4.5	Discussion on Results	127
5.5	Impact Effect of Needle Peeling-off Process	130
5.5.1	Failed Sample Observation	130
5.5.2	Numerical Model	130
5.5.3	Effect of Impact Speed	132
5.5.4	Effect of Substrate Penetration	134
5.6	Summary	135
	References	137
6	Multi-needle Peeling	139
6.1	Introduction	139
6.2	Mechanical Model of Multi-needle Peeling-off	140
6.2.1	Model Description	140
6.2.2	Boundary and Continuity Conditions	142
6.2.3	Determination of Integration Constants	144
6.3	Competing Fracture Model of Chip-Adhesive-Substrate Structure	147
6.3.1	Modeling of Competing Fracture Behavior	147
6.4	Analysis of Bending Normal Stress and ERR of Interfacial Peeling	151
6.4.1	Analysis of Bending Normal Stress	151
6.4.2	Analysis of ERR of Interfacial Peeling	154
6.5	Effect of Chip Geometry on Competing Fracture Behavior	156
6.5.1	Effect of Chip Thickness	156
6.5.2	Effect of Chip Length	158

- 6.6 Experimental Validation 160
 - 6.6.1 Experimental System 160
- 6.7 Summary 162
- References 163
- 7 Conformal Peeling 165
 - 7.1 Introduction 165
 - 7.2 Modeling of Conformal Peeling for Multilayer Structure 166
 - 7.3 Effect of Material Properties and Geometric Size 174
 - 7.3.1 Effect of Young’s Modulus of Device Layer 174
 - 7.3.2 Effect of Young’s Modulus of Adhesive Layer 176
 - 7.3.3 Effect of Device Thickness 179
 - 7.3.4 Effect of Substrate Thickness 181
 - 7.3.5 Selection of Device Thickness 183
 - 7.3.6 Selection of Substrate Thickness 185
 - 7.4 Effects of Process Parameters 186
 - 7.4.1 Effect of Peel Radius 186
 - 7.4.2 Effect of Conformal Angle 186
 - 7.4.3 Effect of Substrate Tension 187
 - 7.5 Experimental Determination of Adhesive Fracture Energy 189
 - 7.6 Design of Peel Blade and Its Application 194
 - 7.6.1 Optimal Design of Peel Blade 194
 - 7.6.2 Experimental Validation 195
 - 7.7 Summary 198
 - References 199
- 8 Laser Lift-off 201
 - 8.1 Introduction 201
 - 8.2 Laser-Induced Interfacial Reaction (LIIR) 202
 - 8.2.1 Band Gap 203
 - 8.2.2 Laser Wavelength 204
 - 8.2.3 Laser Fluence 204
 - 8.2.4 Laser Irradiation Time 205
 - 8.2.5 Laser Scanning Overlap 205
 - 8.2.6 Physical and Chemical Properties of Material 206
 - 8.3 Experimental Study of LLO Mechanism of Ultra-thin PI Film from Glass Carrier 206
 - 8.3.1 Experimental Procedure 206
 - 8.3.2 Optical Phenomena Observed After Laser Irradiation 208
 - 8.3.3 Effects of ART and PI Film Thickness on Threshold Fluence 210
 - 8.3.4 Typical SEM Images of PI/Glass Interface 212
 - 8.3.5 Effects of Laser Fluence and ART on Interface Adhesion Strength 214

8.3.6	Analysis of Separation Mode	216
8.3.7	Analysis of Bubble Height	219
8.3.8	Analysis of Process Window	221
8.4	Summary	221
	References	222
9	Vacuum-Based Picking-up and Placing-on	227
9.1	Introduction	227
9.2	Vacuum-Based Chip Picking-up Process	228
9.2.1	Mechanical Model	228
9.2.2	Boundary and Continuity Conditions	232
9.2.3	Determination of Integration Constants	234
9.2.4	Determination of Picking-up Criterion	235
9.2.5	Effect of Ratio of Adhesive Length to Chip Length	236
9.2.6	Effect of Ratio of VAP Below Substrate	238
9.2.7	Effect of Crack Propagation	240
9.2.8	Effects of Properties of Chip and Substrate Layers	242
9.2.9	Prediction of Chip Picking-up	245
9.2.10	Design of Chip Picking-up	246
9.3	R2R Process with Low Interfacial Residual Stress	248
9.3.1	Temperature and Force-Induced Misfits in R2R Processing	248
9.3.2	Interfacial Stress Related to Structures and Processes	251
9.3.3	Material Selection and Structural Optimization of Film-on-Substrate System	255
9.3.4	Co-optimization on Material, Structure, and Process	260
9.4	Thermal-Pressing Consolidation in Chip Placing-on Process	262
9.4.1	LWT-Based Mechanical Model	262
9.4.2	Equilibrium Equations and Solution Strategy	265
9.4.3	Boundary Conditions	268
9.4.4	Numerical Approach	268
9.4.5	Mechanism of Ultra-thin Chip Warpage	271
9.4.6	Effects of Structure Dimensions and Materials	271
9.4.7	Experimental Verification	273
9.5	Summary	276
	References	277
	Appendix	281