

Contents

1	Introduction	1
1.1	Motivation and Challenges	2
1.1.1	High Throughput	3
1.1.2	Low Latency	3
1.1.3	High Code Rates	5
1.2	Objectives, Outline and Contribution	6
2	Turbo-Codes	11
2.1	Encoding	12
2.1.1	Transmission System Model	12
2.1.2	Turbo-Code Encoder	14
2.1.3	Constituent Encoding: RSC Encoder	14
2.1.4	Trellis	15
2.1.5	LTE Turbo-Encoding and Rate Matching	16
2.2	Decoding	18
2.2.1	General Turbo-Code Decoder	18
2.2.2	Constituent Code Decoding	19
2.2.3	Windowing	20
2.3	Decoder Architectures	22
2.3.1	Design Space	22
2.3.2	Architecture Archetypes	26
2.4	Summary	30

3	Bit-level Considerations	31
3.1	Bit-level Pipelined ACS-Operations	32
3.1.1	Bit-level Pipelined ACS-Operations in MAP Decoding	33
3.1.2	Unsigned CS Number Representation	33
3.1.3	2's Complement CS Number Representation	34
3.2	Bit-level Pipelined XMAP Decoder Architecture	37
3.2.1	Pipeline registers	37
3.2.2	Recursion unit architecture	38
3.3	Case Study	38
4	Advanced Iteration Control Techniques	41
4.1	On-the-fly CRC	42
4.1.1	Latency considerations	44
4.1.2	On-the-fly CRC Calculation Scheme	49
4.1.3	Hardware Architecture and Case Study	53
4.1.4	Silicon Case Study	56
4.2	Iteration Balancing	58
4.2.1	Iteration Balancing for a Single Decoder	59
4.2.2	Iteration Balancing Over Multiple Parallel Decoders	64
4.2.3	Conclusion	68
5	Exploiting Puncturing Patterns	69
5.1	Trellis Compression	70
5.1.1	Compression of RFTSs	71
5.1.2	Applicability to Different Turbo-Code Decoder Architectures	73
5.1.3	Turbo-Code Decoder Architecture with Trellis Compression	74
5.2	Improving the Decoding of Small Code Blocks at High Code Rates	79
5.2.1	Investigations on the Residual Error Distribution	79
5.2.2	Exploiting the Critical Positions	81
5.2.3	Parallel Improved Forced Symbol Decoding	83
5.3	Simulative Evaluation	85
5.3.1	Improved Flip-and-Check	85
5.3.2	Parallel Improved Forced Symbol Decoding	87
5.3.3	Combined Flip-and-Check and Forced Symbol Decoding	87
5.4	Hardware Architecture Case Study	88

6 Conclusion	99
7 Zusammenfassung	101
A Channel Coding	109
A.1 General Terms	109
A.2 Convolutional Codes	113
A.2.1 Encoding	114
A.2.2 Trellis	115
A.2.3 Terminated Convolutional Codes	116
B APP Decoding	121
B.1 The BCJR Algorithm	121
B.2 The Log-MAP Algorithm	124
B.2.1 Soft Output	125
B.2.2 Branch Metrics	126
B.2.3 Alpha and Beta Recursions	128
B.2.4 Log-MAP Variations	128
Acronyms	131
Bibliography	135
List of Figures	143
List of Tables	147
List of Algorithms	149