

Contents

About the Editors	XI
Foreword.....	XIII

Part I: System Design

1 Digital System Design.....	3
1.1 Main processor Units and Instruction sets	3
1.1.1 Main Units.....	3
1.1.2 Instruction Set and Instruction Formats	5
1.1.3 Addressing Modes.....	6
1.2 ASMs for Processor instructions	8
1.3 Data Path Design	15
1.3.1 Combined Functional ASM	15
1.3.2 Process Table and Connection Graph	19
1.3.3 Graph of Incompatibility. Main MUXes and Direct Connections.....	24
1.4 Control Unit Design.....	28
1.4.1 Transformation of Functional ASM into Structural ASM.....	28
1.4.2 Synthesis the Finite State Machine (FSM) from ASM.....	32
1.4.3 Synthesis of Control Unit (FSM) for Processor	34
1.4.4 Encoding of Inputs of MUXes	38
1.5 Conclusions	39
References	41
2 Rectangular Function $\Pi(x)$ and Its Application for Description of Some Logical Devices Operation.....	43
2.1 Introduction	43
2.2 Logic Operations on Rectangular Functions.....	44
A. Logic Sum.....	44
B. Logic Product.....	44
C. Negation.....	45

D. EX-OR (logic inequality)	45
E. Binary Counters	46
2.3 Utilization of the Rectangular Functions $\Pi(x)$ for Analysis of Pulse or Frequency Multiplying	47
2.4 Utilizing the Function $\Pi(x)$ for Harmonic Analysis of Digital Sine Wave Generator.....	49
2.4.1 Digital Sine Wave Generator Based on Digital Integrators	49
2.4.2 Digital Sine Wave Generator Based on ROM.....	52
2.5 Conclusions	56
References	57
3 Design and Application of the PLD-based Reconfigurable Devices	59
3.1 Introduction	59
3.2 Evolution of Computer Systems	61
3.3 Architecture and Structure of PLD-Based Computer Systems	63
3.4 Adaptive Logical Network (ALN).....	67
3.5 Problem-Oriented Structures of Digital Devices	70
3.5.1 Functional Blocks with a Floating Point	70
3.5.2 Functional Blocks for Multiplication of Matrixes.....	75
3.5.3 Designing and Realization of Median Filters.....	76
3.5.4 Hemming Adder Realization.....	84
3.6. Verification of Projects by Means of Stands	85
3.7 Reconfigurable Processors	88
3.8 Conclusions	89
References	91
4 Application of Multilevel Design on the Base of UML for Digital System Developing	93
4.1 Introduction	93
4.2 Features of Digital Systems for Real-Time Image Generation.....	94
4.2.1 Estimation of the Complexity of the Standard Rendering Pipeline	94
Scene Manager	94
Modeling Transformation.....	95
Trivial Accept/Reject Classification.....	95
Lighting	96
Viewing Transformation	96
Clipping	96
Division by w and Mapping to 3D Viewport	97
Rasterization.....	97
Estimation of the Complexity of Geometry Calculations.....	98
4.2.2 The Architectural Decisions and Algorithm Approaches for the Real-Time Rendering Systems	98
Pipelined Object-Order Architectures	99

Image-Order Architectures	99
Comparing of Architectures	100
4.3 Designing of Specialized Processors	100
4.3.1 Scene Processor.....	100
4.3.2 Clipping Processor	108
4.4 Application of Runtime Reconfiguration	109
4.5 Application of UML for HDL-Code Creation	110
4.5.1 Example for 2D Clipping Realization.....	112
4.5.2 Fragment of HDL for Scene Processor Simulation.....	114
4.6 Summary and Future Directions.....	116
References	116

Part II: Digital Design with Programmable Logic

5 Logic Synthesis Method of Digital Circuits Designed for Implementation with Embedded Memory Blocks of FPGAs	121
5.1 Introduction	121
5.2 Decomposition of Boolean Functions.....	122
5.2.1 Functional Decomposition	122
5.2.2 Decomposition into EMB Blocks	125
5.2.3 Parallel Decomposition	126
5.2.4 Balanced Decomposition	128
5.3 Sequential Circuits Synthesis	130
5.3.1 Basic Information.....	131
5.3.2 Implementation of Finite State Machines in FPGA's	132
5.3.3 States Encoding.....	133
5.3.4 Construction of Partition P_G	136
5.3.5 Application of the Method	138
5.4 Experimental Results	139
5.5 Conclusions	142
References	142
6 Efficient Technology Mapping Method for PAL-Based Devices	145
6.1 Introduction	145
6.2 Theoretical Backgrounds	147
6.3 Technology Mapping Algorithm	150
Example.....	152
6.4 Experimental Results	154
6.5 Conclusions	157
References	157
Appendix	159

7 Reliable FPGA-Based Systems Out of Unreliable Automata:	
Multi-version Design Using Genetic Algorithms	165
7.1 Introduction	165
7.2 External and Internal Design Diversity	167
7.3 Partially Definite and Partially Correct Automata.....	170
7.4 Reliability of Digital Systems Out of Unreliable Automata.....	173
7.5 Designing Digital Systems Out of Unreliable Automata.....	176
7.5.1 General GA-Based Approach	176
7.5.2 Phase 1: Obtaining a System Model	178
7.5.3 Phase 2: Increasing the Reliability of Digital Systems Out of Unreliable Automata.....	180
7.5.4 Phase 3: Development of Switching Subsystem	182
7.5.5 Implementation	183
7.6 Experimental Application.....	184
7.7 Conclusions	190
References	191
8 Synthesis of Compositional Microprogram Control Unit with Dedicated Area of Inputs.....	193
8.1 Introduction	193
8.2 Background of CMCU	194
8.3 Synthesis of CMCU with Dedicated Area of Inputs.....	197
8.4 Optimization of Compositional Microprogram Control Unit with the Dedicated Input Area.....	208
8.5 Conclusions	213
References	213
9 PeNLogic – System for Concurrent Logic Controllers Design.....	215
9.1 Introduction	215
9.2 PeNLogic System	216
9.2.1 Petri Net Modeling of Concurrent Controllers.....	216
An Example.....	217
9.2.2 Analysis of Petri Net.....	218
9.2.3 HDL Modeling, Simulation and Synthesis	220
VHDL Modeling	220
Verilog Modeling	221
9.2.4 Petri Nets Decomposition	221
Decomposition into SM-Components	223
Verilog Modeling and Synthesis	224
9.2.5 Direct Mapping into Netlist	226
9.3 Conclusions	227
References	227

Part III: Testing, Modeling and Signal Processing

10	Methods of Signals Processing in Radio Access Networks	231
10.1	General Information	231
10.2	Specific Features of Radio Access at Physical Level	233
10.2.1	General Description of Physical Processes at Radio Access	233
10.2.2	Space-Time Access Method.....	235
10.2.3	Polarization in Access Tasks.....	239
10.2.4	Adaptation in the Tasks of Access	241
10.2.5	Suppression (Rejection) of Interference. Adaptive Antenna Arrays and Adaptive Interference Cancellers.....	241
10.2.6	Control of Multipath Effect in Access Radio Lines	246
10.2.7	Space-Time Coding.....	250
10.3	Recommendations on Practical Use of Signal Processing Algorithms	252
10.3.1	Formalization of Kalman-Bucy Algorithm	252
10.3.2	Recommendations on Planning of Estimation Algorithms ...	253
10.3.3	Program of Estimation Calculation with the Help of FKB....	256
10.3.4	Recommendations for Designing Adaptive Noise Compensators.....	257
10.3.5	Recommendations for Planning Adaptive Antenna Arrays...	258
10.4	Conclusions	260
	References	261
11	Recursive Code Scales for Moving Converters.....	263
11.1	Pseudo-Random Code Scales	263
11.1.1	Pseudo-Random Code Scales for Converters of Angular Movings	263
11.1.2	Pseudo-Random Code Scales for Converters of Linear Moving.....	267
11.2	Composite Code Scales	269
11.2.1	Composite Code Scales for Converters of Angular Moving	269
11.2.2	Composite Code Scales for Converters of Linear Moving....	272
11.3	Placing of Reading Elements on a Recursive Code Scale	274
11.3.1	Algorithm of Placing of Reading Elements on a Recursive Code Scale.....	275
11.3.2	Reading Elements Location on the Pseudo-Random Code Scale with a Constant Step	277
11.3.3	Reading Elements Locations on the Composite Code Scale with a Constant Step.....	280
11.4	Correcting Possibilities of Recursive Code Scales	283
11.5	Conclusions	286
	References	288

12 Infrastructure Intellectual Property for SoC Simulation and Diagnosis Service.....	289
12.1 Infrastructure IP	289
12.2 The Theoretical Foundations of Deductive Fault Analysis	293
12.3 Deductive Components Synthesis for Soc Functions	295
12.4 Structure Models of Simulator Primitives	301
12.5 Algebra-Logical Fault Diagnosis Method	307
12.6 Simulation for Diagnosis Refinement	310
12.7 Structure-Logical Fault Diagnosis Method.....	313
12.8 Vector-Logical Diagnosis Method by the Fault Detection Table	316
12.9 Algebra-Logical Memory Repair Method	320
12.10 Conclusions	326
References	328
13 Evolutionary Test Generation Methods for Digital Devices.....	331
13.1 Genetic Algorithms and Their Modifications.....	331
13.1.1 Parents Selection	332
13.1.2 Crossover Operators.....	333
13.1.3 Mutation.....	334
13.2 Genetic Test Generation Algorithm for Digital Circuits	335
13.2.1 Test Generation Genetic Algorithms for Combinational Circuits	336
13.2.2 Test Generation Genetic Algorithms for Sequential Circuits	339
13.2.3 Problem-Oriented Fitness Functions for Test Generation....	342
13.2.4 GA Test Generation Implementation	345
13.3 Distributed Test Generation Methods.....	346
13.3.1 GA Parallelization.....	346
13.3.2 Parallel Test Generation Method Based on the “Master-Slave” Model	348
13.3.3 Distributed Fault Simulation	349
13.3.4 Distributed Test Generation Based on the “Model of Islands”	351
13.3.5 Implementation and Experimental Investigations of Distributed Genetic Algorithms of Test Generation and Simulation	352
13.6 Hierarchical GA of Test Generation for Highly Sequential Circuits	353
13.7 Genetic Programming in Test Generation of Microprocessor Systems.....	357
13.8 Conclusions	361
References	361
Index.....	363