

Table of Contents

FPGA-Based High-Speed Authenticated Encryption System	1
<i>Michael Muehlberghuber, Christoph Keller, Frank K. Gürkaynak, and Norbert Felber</i>	
A Smart Memory Accelerated Computed Tomography Parallel Backprojection	21
<i>Qiuling Zhu, Larry Pileggi, and Franz Franchetti</i>	
Trinocular Stereo Vision Using a Multi Level Hierarchical Classification Structure	45
<i>Andy Motten, Luc Claesen, and Yun Pan</i>	
Spatially-Varying Image Warping: Evaluations and VLSI Implementations	64
<i>Pierre Greisen, Michael Schaffner, Danny Luu, Val Mikos, Simon Heinzle, Frank K. Gürkaynak, and Aljoscha Smolic</i>	
An Ultra-Low-Power Application-Specific Processor with Sub- V_T Memories for Compressed Sensing	88
<i>Jeremy Constantin, Ahmed Dogan, Oskar Andersson, Pascal Meinerzhagen, Joachim Rodrigues, David Atienza, and Andreas Burg</i>	
Configurable Low-Latency Interconnect for Multi-core Clusters	107
<i>Giulia Beanato, Igor Loi, Giovanni De Micheli, Yusuf Leblebici, and Luca Benini</i>	
A Hexagonal Processor and Interconnect Topology for Many-Core Architecture with Dense On-Chip Networks	125
<i>Zhibin Xiao and Bevan Baas</i>	
Fault-Tolerant Techniques to Manage Yield and Power Constraints in Network-on-Chip Interconnections	144
<i>Anelise Kologeski, Caroline Concatto, Fernanda Lima Kastensmidt, and Luigi Carro</i>	
On the Automatic Generation of Software-Based Self-Test Programs for Functional Test and Diagnosis of VLIW Processors	162
<i>Davide Sabena, Luca Sterpone, and Matteo Sonza Reorda</i>	

SEU-Aware Low-Power Memories Using a Multiple Supply Voltage
Array Architecture 181
Seokjoong Kim and Matthew R. Guthaus

CMOS Implementation of Threshold Gates with Hysteresis 196
Farhad A. Parsan and Scott C. Smith

Simulation and Experimental Characterization of a Unified Memory
Device with Two Floating-Gates 217
*Neil Di Spigna, Daniel Schinke, Srikant Jayanti, Veena Misra, and
Paul Franzon*

Author Index 235