Table of Contents

Process Aware Ultra-High-Speed Hybrid Sensing Technique for Low Power Near-Threshold SRAM 1
Bhupendra Singh Reniwal and Santosh Kumar Vishvakarma

A Novel Design Methodology for High Tuning Linearity and Wide Tuning Range Ring Voltage Controlled Oscillator 10
Gudlavalleti Rajahari, Yashu Anand Varshney, and Subash Chandra Bose

A Low-Power Wideband High Dynamic Range Single-Stage Variable Gain Amplifier 19
Vivek Verma and Chetan D. Parikh

An Ultra-Wideband Baseband Transmitter Design for Wireless Body Area Network 26
R.K. Naga Mahesh, Akash Ganesan, Manchi Pavan Kumar, and Roy P. Paily

Computational Functions' VLSI Implementation for Compressed Sensing 35
Shrirang Korde, Amol Khandare, Raghavendra Deshmukh, and Rajendra Patrikar

A Novel Input Capacitance Modeling Methodology for Nano-Scale VLSI Standard Cell Library Characterization 44
Akhtar W. Alam, Esakkimuthu Dhakshinamoorthy, Prince Mathew, and Narender Ponna

An Area Efficient Wide Range On-Chip Delay Measurement Architecture 49
Rahul Krishnamurthy and G.K. Sharma

10 Gbps Current Mode Logic I/O Buffer 59
Akhil Rathore and Chetan D. Parikh

Kapees: A New Tool for Standard Cell Placement 66
Sameer Pawanekar, Kalpesh Kapoor, and Gaurav Trivedi

Preemptive Test Scheduling for Network-on-Chip Using Particle Swarm Optimization 74
Kanchan Manna, Shailesh Singh, Santanu Chattopadhyay, and Indranil Sengupta

Energy Efficient Array Initialization Using Loop Unrolling with Partial Gray Code Sequence 83
Sumanta Pyne and Ajit Pal

Design and Simulation of Bulk Micromachined Accelerometer for Avionics Application 94
Amit Sharma, Ravindra Mukhiya, S. Santosh Kumar, and B.D. Pant

Performance Analysis of Subthreshold 32-Bit Kogge-Stone Adder for Worst-Case-Delay and Power in Sub-micron Technology 100
Himadri Singh Raghav, Sachin Maheshwari, and Brahmadeo Prasad Singh

Characterization of Logical Effort for Improved Delay 108
Sachin Maheshwari, Himadri Singh Raghav, and Anu Gupta

A Dual Material Double-Layer Gate Stack Junctionless Transistor for Enhanced Analog Performance 118
Ratul Kumar Baruah and Roy P. Paily

An Improved g_m/I_D Methodology for Ultra-Low-Power Nano-Scale CMOS OTA Design 128
Somnath Paul, Abhijit Dana, and Soumya Pandit

An Efficient RF Energy Harvester with Tuned Matching Circuit 138
Sachin Agrawal, Sunil Pandey, Jawar Singh, and P.N. Kondekar

A Modified Gate Replacement Algorithm for Leakage Reduction Using Dual-T_{ox} in CMOS VLSI Circuits 146
Surabhi Singh, Brajesh Kumar Kaushik, and Sudeb Dasgupta

Impact of Fin Width and Graded Channel Doping on the Performance of 22nm SOI FinFET 153
Jose Joseph and Rajendra Patrikar

Power Reduction by Integrated Within_Clock_Power Gating and Power Gating (WCPG_in_PG) 160
Debanjali Nath, Priyanka Choudhury, and Sambhu Nath Pradhan

Design and Analysis of a Novel Noise Cancelling Topology for Common Gate UWB LNAs 169
Mohd Anwar, Syed Azeemuddin, and Mohammed Zafar Ali Khan

A Combined CMOS Reference Circuit with Supply and Temperature Compensation 177
Madhusoodan Agrawal and Alpana Agarwal

Convex Optimization of Energy and Delay Using Logical Effort Method in Deep Sub-micron Technology 185
Sachin Maheshwari, Rameez Raza, Pramod Kumar, and Anu Gupta

A Cache-Aware Strategy for H.264 Decoding on Multi-processor Architectures 194
Arani Bhattacharya, Ansuman Banerjee, Susmita Sur-Kolay, Prasenjit Basu, and Bhaskar J. Karmakar

Random-LRU: A Replacement Policy for Chip Multiprocessors 204
Shirshendu Das, Nagaraju Polavarapu, Prateek D. Halwe, and Hemangee K. Kapoor

Analysis of Crosstalk Deviation for Bundled MWCNT with Process Induced Height and Width Variations 214
Jainender Kumar, Manoj Kumar Majumder, Brajesh Kumar Kaushik, and Sudeb Dasgupta

Congestion Balancing Global Router 223
Shyamapada Mukherjee, Jibesh Patra, and Suchismita Roy

CMOS ASIC Design of a High Performance Digital Fuzzy Processor That Can Compute on Arbitrary Membership Functions 233
Anirban Guha and Shubhajit Roy Chowdhury

Variation Robust Subthreshold SRAM Design with Ultra Low Power Consumption 242
Saima Cherukat and Vineet Sahula

Modeling of High Frequency Out-of-Plane Single Axis MEMS Capacitive Accelerometer 249
Prashant Singh, Pooja Srivastava, Ram Mohan Verma, and Saurabh Jaiswal

CPK Based IO AC Timing Closure to Reduce Yield Loss and Test Time 257
Sandip Ghosh and Rohit Srivastava

Optimization of Underlap FinFETs and Its SRAM Performance Projections Using High-k Spacers 267
Pankaj Kr. Pal, Brajesh Kumar Kaushik, and Sudeb Dasgupta

On-Chip Dilution from Multiple Concentrations of a Sample Fluid Using Digital Microfluidics 274
Sudip Roy, Bhargab B. Bhattacharya, Sarmishtha Ghoshal, and Krishnendu Chakrabarty

Automatic Test Bench Generation and Connection in Modern Verification Environments: Methodology and Tool 284
Rohit Srivastava, Gaurav Gupta, Sarvesh Patankar, and Nandini Mudgil

A Methodology for Early and Accurate Analysis of Inrush and Latency Tradeoffs during Power-Domain Wakeup 294
Vipul Singhal, Ayon Dey, Suresh Mallala, and Somshubhra Paul

Fault Aware Dynamic Adaptive Routing Using LBDR 304
Rimpy Bishnoi, Vijay Laxmi, Manoj Singh Gaur, and Mohit Baskota

Architectural Level Sub-threshold Leakage Power Estimation of SRAM Arrays with Its Peripherals 312
Nupur Navlakha, Lokesh Garg, Dharmendar Boolchandani, and Vineet Sahula

On Designing Testable Reversible Circuits Using Gate Duplication 322
Joyati Mondal, Debesh Kumar Das, Dipak Kumar Kole, Hafizur Rahaman, and Bhargab B. Bhattacharya

Circuit Transient Analysis Using State Space Equations 330
Kai Chi Alex Lam and Mark Zwolinski

3D CORDIC Algorithm Based Cartesian to Spherical Coordinate Converter 337
Anita Jain and Kavita Khare

Level-Accurate Peak Activity Estimation in Combinational Circuit Using BILP 345
Jaynarayan T. Tudu, Deepak Malani, and Virendra Singh

Design and Optimization of a 2x2 Directional Microstrip Patch Antenna 353
Cerin Ninan, Chandra Shekhar, and M. Radhakrishna

A New Method for Route Based Synthesis and Placement in Digital Microfluidic Biochips 361
Pranab Roy, Samadrita Bhattacharya, Hafizur Rahaman, and Parthasarathi Dasgupta

Defect Diagnosis of Digital Circuits Using Surrogate Faults 376
Chidambaram Alagappan and Vishwani D. Agrawal

Author Index 387