## Table of Contents

Session 1: Microprocessor and Implementation	
A Method of Balancing the Global Multi-mode Clock Network in Ultra-large Scale CPU	1
Hardware Architecture for the Parallel Generation of Long-Period Random Numbers Using MT Method	8
MGTE: A Multi-level Hybrid Verification Platform for a 16-Core Processor	16
An Efficient Parallel SURF Algorithm for Multi-core Processor Zhong Liu, Binchao Xing, and Yueyue Chen	27
A Study of Cache Design in Stream Processor	38
Design and Implementation of Dynamically Reconfigurable Token Coherence Protocol for Many-Core Processor	49
Dynamic and Online Task Scheduling Algorithm Based on Virtual Compute Group in Many-Core Architecture	57
ADL and High Performance Processor Design	67
Session 2: Design of Integration Circuit	
The Design of the ROHC Header Compression Accelerator	75
A Hardware Implementation of Nussinov RNA Folding Algorithm Qilong Su, Jiang Jiang, and Yuzhuo Fu	84
A Configurable Architecture for 1-D Discrete Wavelet Transform	92
A Comparison of Folded Architectures for the Discrete Wavelet  Transform	102



A High Performance DSP System with Fault Tolerant for Space Missions	111
Kang Xia, Ao Shen, Yuzhuo Fu, Ting Liu, and Jiang Jiang	111
The Design and Realization of Campus Information Release Platform Based on Android Framework	121
A Word-Length Optimized Hardware Gaussian Random Number Generator Based on the Box-Muller Method	129
Session 3: I/O Interconnect	
DAMQ Sharing Scheme for Two Physical Channels in High Performance Router	138
Yongqing Wang and Minxuan Zhang	
Design and Implementation of Dynamic Reliable Virtual Channel for Network-on-Chip	148
	155
Efficient Broadcast Scheme Based on Sub-network Partition for Many-Core CMPs on Gem5 Simulator	163
A Quick Method for Mapping Cores Onto 2D-Mesh Based Networks on Chip	173
Session 4: Measurement, Verification, and Others	
A Combined Hardware/Software Measurement for ARM Program  Execution Time	185
A Low-Complexity Parallel Two-Sided Jacobi Complex SVD Algorithm and Architecture for MIMO Beamforming Systems	202
A Thermal-Aware Task Mapping Algorithm for Coarse Grain Reconfigurable Computing System	211

	Table of Contents	XIII
DC Offset Mismatch Calibration for Time-Interleaved High-Speed OFDM Receivers		221
A Novel Graph Model for Loop Mapping on Coarse-Reconfigurable Architectures		231
Memristor Working Condition Analysis Based on SPIC Zhuo Bi, Ying Zhang, and Yunchuan Xu	CE Model	242
On Stepsize of Fast Subspace Tracking Methods Zhu Cheng, Zhan Wang, Haitao Liu, and Majid Al		253
Author Index		263