

Contents

1	Introduction	1
1.1	Models of Computation	2
1.2	DEVS Model of Computation	4
1.3	Hardware / Software Co-Design Flow	5
1.4	Remainder of this Thesis	7
2	Discrete Event System Specification	9
2.1	Classic DEVS with Ports and Parallel DEVS Coupled Models	10
2.1.1	Parallel Components	10
2.1.2	Atomic Components	12
2.2	Synthesizable DEVS	16
2.2.1	Output Port Event Bags	16
2.2.2	Confluent Transition Function Output Behaviour . .	24
2.2.3	Component Interconnection	25
2.2.4	Parallel Components	29
2.2.5	Atomic Components	30
2.3	Reconfiguration	37
2.4	Graphical Representation	38
2.4.1	Parallel Components	39
2.4.2	Atomic Components	39
3	Modelling and Validation	43
3.1	Model Creation	45
3.1.1	Model Transformations	45
3.1.2	State-Based Models of Computation	49
3.1.3	Control and Data Flow	51
3.2	Validation of DEVS Models	52
3.3	DEVS MoC Simulation with SystemC	53
3.3.1	Time Representation	54
3.3.2	Event-based Communication Implementation	54
3.3.3	Behaviour Execution	56

3.3.4	Model Elaboration and Simulation	57
3.3.5	Performance Evaluation	63
4	Hardware / Software Co-Design with SynDEVS MoC	69
4.1	Hardware / Software Partitioning	73
4.2	SynDEVS to Hardware Transformation	75
4.2.1	MoC to Hardware Transformation	76
4.2.2	SynDEVS MoC Transformation into VHDL	77
4.2.3	Optimization of Zero-Timeout States	88
4.2.4	Back-Annotation of Resource Utilization	93
4.3	SynDEVS to Software Transformation	96
4.3.1	SynDEVS MoC to C++ Transformation	98
4.3.2	Communication Interface Generation	109
5	Graphical User Interface	119
5.1	SynDEVS Model Editor	120
5.2	SynDEVS MoC SCXML File Format Handling	122
5.3	Arithmetic and Logical Expressions	124
5.4	Expression Parser Implementation	128
5.5	Examples	129
6	Case Studies	131
6.1	Digital Video Interface Controller	131
6.1.1	Time Flow	134
6.1.2	Control Flow	134
6.1.3	Results	135
6.2	Network-based Pong Game	136
6.2.1	SynDEVS Model	138
6.2.2	Results	140
6.3	Cryptographic Accelerator	141
6.3.1	Design Principles	141
6.3.2	Architecture of the Cryptographic System	143
6.3.3	SynDEVS Model of the Cryptographic Main Operations	146
6.3.4	Results	150
7	Summary	157
A	Source Codes	161
A.1	DEVS Component	161
A.2	GPT Example	171

A.3	UART Receiver (VHDL)	177
A.4	UART Transceiver (C++)	180
B	List of Publications	187
C	List of Supervised Theses	189
	References	191