

Adaptive Techniques for Mixed Signal System on Chip

by

Ayman Fayed

Texas Instruments Inc., Dallas, Texas, U.S.A.

and

Mohammed Ismail

Analog VLSI Lab, Ohio State University Columbus, Ohio, U.S.A.

Contents

Dedication..... v

Preface..... xi

1. Introduction 1

1.1 Categories of Variations in Analog and Mixed Signal ICs..... 2

1.1.1 Circuit Level Variations..... 2

1.1.2 System Level Variations..... 4

1.1.3 Network Level Variations..... 5

1.2 The Essence of Adaptation..... 5

1.3 The Process of Adaptation..... 6

1.4 Book Outline..... 8

2. Adaptive Architectures..... 11

2.1 Automatic Tuning..... 12

2.1.1 Voltage, Current, and Time References..... 16

2.1.2 Electronically Tunable Elements..... 21

2.2 Post Fabrication Tuning..... 35

2.3 Summary..... 36

3. Tunable Elements..... 39

3.1 Voltage-Controlled Transconductors..... 39

3.1.1 A Triode-Based Voltage-Controlled Transconductor... 40

3.1.2	An Improved Voltage-Controlled Transconductor.....	45
3.1.3	Simulations Results.....	48
3.2	Comparators.....	55
3.2.1	Offset Comparators.....	56
3.2.2	A Voltage-Controlled Offset Comparator.....	58
3.2.3	Simulation Results.....	63
3.3	Summary.....	65
4.	On-Chip Resistors and Capacitors.....	67
4.1	Passive Resistors.....	68
4.1.1	Accuracy of Passive Resistors.....	72
4.1.2	Matching Properties of Passive Resistors.....	77
4.2	Passive Capacitors.....	80
4.2.1	Accuracy of Passive Capacitors.....	90
4.2.2	Matching Properties of Passive Capacitors.....	92
4.3	Summary.....	94
5.	A Digital Adaptive Technique for On-Chip Resistors.....	95
5.1	The Calibration Technique.....	97
5.1.1	Variation Range Quantization Concept.....	97
5.1.2	The Resistor Block.....	98
5.1.3	The Algorithm.....	99
5.1.4	Quantifying the Drift.....	103
5.1.5	Tuning Signal Generation.....	104
5.2	Practical Advantages and Limitations.....	107
5.2.1	Accuracy Limitations.....	107
5.2.2	Practical Advantages.....	109
5.2.3	Design Considerations.....	112
5.3	Applications.....	113
5.3.1	A 480 Mbps Transceiver.....	114
5.3.2	A 1.65 Gbps Transceiver.....	117
5.4	Summary.....	118
6.	Equalization.....	121
6.1	Intersymbol Interference.....	121
6.2	Eye Diagrams.....	129
6.3	Equalization Architectures.....	131
6.3.1	The Feed-Forward Architecture.....	133
6.3.2	The Feed-Back Architecture.....	136
6.3.3	The Mixed Feed-Forward Feed-back Architecture.....	139
6.4	Implementation Techniques.....	139

6.5	Summary.....	140
7.	An Analog Adaptive Equalizer for Wire Line Transceivers.....	141
7.1	Motivation.....	142
7.2	Transmission Channel Modeling.....	143
7.3	A Feed-Forward Adaptive Equalizer.....	146
7.3.1	The Forward Equalizer.....	148
7.3.2	The Slicer.....	150
7.3.3	The Reference Signal Generator.....	153
7.3.4	The Band-Pass Filter.....	154
7.3.5	The Differential-Difference Squarer.....	154
7.3.6	The Integrator.....	156
7.4	Simulation Results.....	159
7.5	Measurements Results.....	167
7.6	Summary.....	170
	Bibliography.....	173
	Index.....	177