

# Table of Contents

## Lower Power 1

An Efficient High Frequency and Low Power Analog Multiplier in Current Domain .....	1
<i>Anu Gupta and Subhrojyoti Sarkar</i>	
Design of Push-Pull Dynamic Leaker Circuit for a Low Power Embedded Voltage Regulator .....	10
<i>Biswajit Maity and Pradip Mandal</i>	
Power Modeling of Power Gated FSM and Its Low Power Realization by Simultaneous Partitioning and State Encoding Using Genetic Algorithm .....	19
<i>Priyanka Choudhury and Sambhu Nath Pradhan</i>	

## Analog VLSI Design I

Design and Implementation of a Linear Feedback Shift Register Interleaver for Turbo Decoding .....	30
<i>Rahul Shrestha and Roy Paily</i>	
Low Complexity Encoder for Crosstalk Reduction in <i>RLC</i> Modeled Interconnects .....	40
<i>Gunti Nagendra Babu, Brajesh Kumar Kaushik, Anand Bulusu, and Manoj Kumar Majumder</i>	
Analog Performance Analysis of Dual-k Spacer Based Underlap FinFET .....	46
<i>Ashutosh Nandi, Ashok K. Saxena, and Sudeb Dasgupta</i>	

## Test and Verification I

Implementation of Gating Technique with Modified Scan Flip-Flop for Low Power Testing of VLSI Chips .....	52
<i>R. Jayagowri and K.S. Gurumurthy</i>	
Post-bond Stack Testing for 3D Stacked IC .....	59
<i>Surajit Kumar Roy, Dona Roy, Chandan Giri, and Hafizur Rahaman</i>	
Translation Validation for PRES+ Models of Parallel Behaviours via an FSMD Equivalence Checker .....	69
<i>Soumyadip Bandyopadhyay, Kunal Banerjee, Dipankar Sarkar, and Chittaranjan R. Mandal</i>	

## Design Techniques I

Design of High Speed Vedic Multiplier for Decimal Number System . . . . .	79
<i>Prabir Saha, Arindam Banerjee, Anup Dandapat, and Partha Bhattacharyya</i>	
An Efficient Test Design for CMPs Cache Coherence Realizing MESI Protocol . . . . .	89
<i>Mamata Dalui and Biplob K. Sikdar</i>	
An Efficient High Speed Implementation of Flexible Characteristic-2 Multipliers on FPGAs . . . . .	99
<i>Debapriya Basu Roy and Debdeep Mukhopadhyay</i>	

## Algorithms and Applications I

Arithmetic Algorithms for Ternary Number System . . . . .	111
<i>Subrata Das, Partha Sarathi Dasgupta, and Samar Sensarma</i>	
SOI MEMS Based Over-Sampling Accelerometer Design with $\Delta\Sigma$ Output . . . . .	121
<i>Dushyant Juneja, Sougata Kar, Procheta Chatterjee, and Siddhartha Sen</i>	
Design Optimization of a Wide Band MEMS Resonator for Efficient Energy Harvesting . . . . .	129
<i>Goutam Rana, Samir Kumar Lahiri, and Chirasree Roychaudhuri</i>	

## Lower Power II

Ultra-Low Power Sub-threshold SRAM Cell Design to Improve Read Static Noise Margin . . . . .	139
<i>Chandrabhan Kushwah and Santosh K. Vishvakarma</i>	
Workload Driven Power Domain Partitioning . . . . .	147
<i>Arun Dobriyal, Rahul Gonnabattula, Pallab Dasgupta, and Chittaranjan R. Mandal</i>	
Implementation of a New Offset Generator Block for the Low-Voltage, Low-Power Self Biased Threshold Voltage Extractor Circuit . . . . .	156
<i>Rituparna Dasgupta, Dipankar Saha, Jagannath Samanta, Sayan Chatterjee, and Chandan Kumar Sarkar</i>	

## Analog VLSI Design II

A High Speed, Low Jitter and Fast Acquisition CMOS Phase Frequency Detector for Charge Pump PLL . . . . .	166
<i>Manas Kumar Hati and Tarun Kanti Bhattacharyya</i>	

ILP Based Approach for Input Vector Controlled (IVC) Toggle Maximization in Combinational Circuits .....	172
<i>Jaynarayan T. Tudu, Deepak Malani, and Virendra Singh</i>	

Comparison of OpAmp Based and Comparator Based Switched Capacitor Filter .....	180
<i>Manodipan Sahoo and Bharadwaj Amratur</i>	

## Test and Verification II

Effect of Malicious Hardware Logic on Circuit Reliability .....	190
<i>Sanjay Burman, Ayan Palchaudhuri, Rajat Subhra Chakraborty, Debdeep Mukhopadhyay, and Pranav Singh</i>	

A Modified Scheme for Simultaneous Reduction of Test Data Volume and Testing Power .....	198
<i>Sruthi P.R. and M. Nirmala Devi</i>	

Reusable and Scalable Verification Environment for Memory Controllers .....	209
<i>Kiran Kumar Abburi, Siva Subrahmanyam Evani, Sajeev Thomas, and Anup Aprem</i>	

## Design Techniques II

Design of a Fault-Tolerant Conditional Sum Adder .....	217
<i>Atin Mukherjee and Anindya Sundar Dhar</i>	

SEU Tolerant Robust Latch Design .....	223
<i>Mohammed Shayan, Virendra Singh, Adit D. Singh, and Masahiro Fujita</i>	

Design of Content Addressable Memory Architecture Using Carbon Nanotube Field Effect Transistors .....	233
<i>Debaprasad Das, Avisek Sinha Roy, and Hafizur Rahaman</i>	

## Algorithms and Applications II

High-Speed Unified Elliptic Curve Cryptosystem on FPGAs Using Binary Huff Curves .....	243
<i>Ayantika Chatterjee and Indranil Sengupta</i>	

A $4 \times 20$ Gb/s $2^9$ -1 PRBS Generator for Testing a High-Speed DAC in 90nm CMOS Technology .....	252
<i>Mahendra Sakare, Mohit Singh, and Shalabh Gupta</i>	

VLSI Architecture for Bit Parallel Systolic Multipliers for Special Class of GF ( $2^m$ ) Using Dual Bases . . . . .	258
<i>Hafizur Rahaman, Jimson Mathew, A.M. Jabir, and Dhiraj K. Pradhan</i>	
<b>Emerging Technologies</b>	
A Synthesis Method for Quaternary Quantum Logic Circuits . . . . .	270
<i>Sudhindu Bikash Mandal, Amlan Chakrabarti, and Susmita Sur-Kolay</i>	
On the Compact Designs of Low Power Reversible Decoders and Sequential Circuits . . . . .	281
<i>Lafifa Jamal, Md. Masbaul Alam Polash, M.A. Mottalib, and Hafiz Md. Hasan Babu</i>	
Delay Uncertainty in Single- and Multi-Wall Carbon Nanotube Interconnects . . . . .	289
<i>Debaprasad Das and Hafizur Rahaman</i>	
<b>Algorithms and Applications III</b>	
A Fast FPGA Based Architecture for Sobel Edge Detection . . . . .	300
<i>Santanu Halder, Debotosh Bhattacharjee, Mita Nasipuri, and Dipak Kumar Basu</i>	
Speech Processor Design for Cochlear Implants . . . . .	307
<i>Arun Kumarappan and P.V. Ramakrishna</i>	
An Efficient Technique for Longest Prefix Matching in Network Routers . . . . .	317
<i>Rekha Govindaraj, Indranil Sengupta, and Santanu Chattopadhyay</i>	
<b>NoC and Physical Design</b>	
A Faster Hierarchical Balanced Bipartitioner for VLSI Floorplans Using Monotone Staircase Cuts . . . . .	327
<i>Bapi Kar, Susmita Sur-Kolay, Sridhar H. Rangarajan, and Chittaranjan R. Mandal</i>	
Test Data Compression for NoC Based SoCs Using Binary Arithmetic Operations . . . . .	337
<i>Sanga Chaki and Chandan Giri</i>	
Particle Swarm Optimization Based BIST Design for Memory Cores in Mesh Based Network-on-Chip . . . . .	343
<i>Bibhas Ghoshal, Subhadip Kundu, Indranil Sengupta, and Santanu Chattopadhyay</i>	

## Poster Presentation

An Efficient Multiplexer in Quantum-dot Cellular Automata . . . . .	350
<i>Bibhash Sen, Manojit Dutta, Divyam Saran, and Biplab K. Sikdar</i>	
Integrated Placement and Optimization Flow for Structured and Regular Logic . . . . .	352
<i>Vikram Singh Saun, Suman Chatterjee, and Anand Arunachalam</i>	
A Novel Symbol Estimation Algorithm for LTE Standard . . . . .	354
<i>K Kalyani and S. Rajaram</i>	
Impact of Dummy Poly on the Process-Induced Mechanical Stress Enhanced Circuit Performance . . . . .	357
<i>Naushad Alam, Bulusu Anand, and Sudeb Dasgupta</i>	
A Novel Approach to Voltage-Drop Aware Placement in Large SoCs in Advanced Technology Nodes . . . . .	360
<i>Biswajit Patra, Santan Chattopadhyay, and Amlan Chakrabarti</i>	
Design and Implementation of Efficient Vedic Multiplier Using Reversible Logic . . . . .	364
<i>P. Saravanan, P. Chandrasekar, Livya Chandran, Nikilla Sriram, and P. Kalpana</i>	
Design of Combinational and Sequential Circuits Using Novel Feedthrough Logic . . . . .	367
<i>Sauvagya Ranjan Sahoo and Kamala Kanta Mahapatra</i>	
Efficient FPGA Implementation of Montgomery Multiplier Using DSP Blocks . . . . .	370
<i>Arpan Mondal, Santosh Ghosh, Abhijit Das, and Dipanwita Roy Chowdhury</i>	
Independent Gate SRAM Based on Asymmetric Gate to Source/Drain Overlap-Underlap Device FinFET . . . . .	373
<i>Naveen Kaushik, Brajesh Kumar Kaushik, Davinder Kaur, and Manoj Kumar Majumder</i>	
VLSI Architecture for Spatial Domain Spread Spectrum Image Watermarking Using Gray-Scale Watermark . . . . .	375
<i>Sudip Ghosh, Somsubhra Talapatra, Debasish Mondal, Navonil Chatterjee, Hafizur Rahaman, and Santi P. Maitty</i>	
A Photonic Network on Chip with CDMA Links . . . . .	377
<i>Soumyajit Poddar, Prasun Ghosal, Priyajit Mukherjee, Suman Samui, and Hafizur Rahaman</i>	

Simulation Study of an Ultra Thin Body Silicon On Insulator Tunnel Field Effect Transistor .....	379
<i>Partha Sarathi Gupta, Sayan Kanungo, Hafizur Rahaman, and     Partha Sarathi Dasgupta</i>	
Routing in NoC on Diametrical 2D Mesh Architecture .....	381
<i>Prasun Ghosal and Tuhin Subhra Das</i>	
<b>Invited Talk</b>	
Reversible Circuits: Recent Accomplishments and Future Challenges for an Emerging Technology (Invited Paper) .....	383
<i>Rolf Drechsler and Robert Wille</i>	
Power Problems in VLSI Circuit Testing .....	393
<i>Farhana Rashid and Vishwani D. Agrawal</i>	
<b>Author Index .....</b>	407