

Contents

Preface *xi*

1	The Future of CMOS: More Moore or a New Disruptive Technology? 1
	<i>Nazek El-Atab and Muhammad M. Hussain</i>
1.1	FinFET Technology 2
1.1.1	State-of-the-Art FinFETs 3
1.1.1.1	FinFET with Si Channel 3
1.1.1.2	FinFET with High-Mobility Material Channel 4
1.1.1.3	FinFET with TMD Channel 5
1.1.1.4	SOI versus Bulk FinFET 5
1.1.2	Industrial State 6
1.1.3	Challenges and Limitations 7
1.2	3D Integrated Circuit Technology 8
1.2.1	Research State 9
1.2.1.1	Thermal Management 9
1.2.1.2	Through-silicon-vias 9
1.2.1.3	Bonding in 3D IC 10
1.2.1.4	Test and Yield 12
1.2.2	Industrial State 12
1.2.3	Challenges and Limitations 13
1.3	Neuromorphic Computing Technology 13
1.3.1	State-of-the-Art Nonvolatile Memory as a Synapse 14
1.3.1.1	Phase Change Memory 15
1.3.1.2	Conductive-Bridging RAM 16
1.3.1.3	Filamentary RRAM 17
1.3.2	Research Programs and Industrial State of Neuromorphic Computing 18
1.4	Quantum Computing Technology 19
1.4.1	Quantum Bit Requirement 20
1.4.2	Research State 20
1.4.2.1	Spin-Based Qubits 20
1.4.3	Superconducting Circuits for Quantum Information 21
1.4.4	Industry State 22
1.4.5	Challenges and Limitations to Quantum Computing 23
	References 23

2	Nanowire Field-Effect Transistors	33
	<i>Debarghya Sarkar, Ivan S. Esqueda, and Rehan Kapadia</i>	
2.1	General Scaling Laws Leading to Nanowire Architectures	33
2.1.1	Scaling of Planar Devices and Off-state Leakage Current	33
2.1.2	FinFET and UTB Devices for Improved Electrostatics	35
2.1.3	Nanowires as the Ultimate Limit of Electrostatic Control	37
2.1.4	Quantum Effects	39
2.1.5	Drive Current	43
2.2	Nanowire Growth and Device Fabrication Approaches	43
2.2.1	Bottom-up VLS Growth	43
2.2.2	Top-down Oxidation	45
2.3	State-of-the-Art Nanowire Devices	45
2.3.1	Silicon Devices	45
2.3.2	III–V Devices	46
	References	49
3	Two-dimensional Materials for Electronic Applications	55
	<i>Haimeng Zhang and Han Wang</i>	
3.1	2D Materials Transistor and Device Technology	56
3.1.1	Operation and Characteristics of 2D-Materials-Based FETs	57
3.1.2	Ambipolar Property of Graphene	57
3.1.3	Important Figures of Merit	58
3.1.3.1	$I_{\text{on}}/I_{\text{off}}$ Ratio	58
3.1.3.2	Subthreshold Swing	59
3.1.3.3	Cutoff Frequency and Maximum Frequency of Oscillation	59
3.1.3.4	Minimum Noise Figure	60
3.1.4	Device Optimization	61
3.1.4.1	Mobility Engineering	61
3.1.4.2	Current Saturation	62
3.1.4.3	Metal Contact	63
3.2	Graphene Electronics for Radiofrequency Applications	64
3.2.1	Experimental Graphene RF Transistors	65
3.2.2	Graphene-Based Integrated Circuits	67
3.2.2.1	Graphene Ambipolar Devices	67
3.2.2.2	Graphene Oscillators	73
3.2.2.3	Graphene RF Receivers	73
3.2.2.4	Graphene Electromechanical Devices: Resonators and RF Switches	74
3.3	MoS ₂ Devices for Digital Application	76
3.3.1	Experimental MoS ₂ Transistors	77
3.3.2	MoS ₂ -Based Integrated Circuits	78
3.3.2.1	Direct-Coupled FET Logic Circuits	78
3.3.2.2	Logic Gates	79
3.3.2.3	A Static Random Access Memory Cell based on MoS ₂	82
3.3.2.4	Ring Oscillators based on MoS ₂	82
3.3.2.5	Microprocessors based on MoS ₂	85
	References	87

4	Integration of Germanium into Modern CMOS: Challenges and Breakthroughs	91
	<i>Wonil Chung, Heng Wu, and Peide D. Ye</i>	
4.1	Introduction	91
4.2	Junction Formation for Germanium MOS Devices	92
4.2.1	Charge Neutrality Level and Fermi Level Pinning	92
4.2.2	Metal/Ge Contacts	93
4.2.2.1	Alleviation of FLP	93
4.2.2.2	Metal/n-Ge Contact	93
4.2.2.3	Recessed Contact Formation	94
4.3	Process Integration for Ge MOS Devices	97
4.3.1	Interface Engineering Issues	97
4.3.2	Various Gate Stack Combinations for Ge MOSFET	97
4.3.2.1	GeO _x -Free Gate Stack with ALD High-κ	98
4.3.2.2	Silicon Interfacial Layer Passivation	99
4.3.2.3	Germanium (Oxy)Nitridation	99
4.3.2.4	GeO ₂ -Based Gate Stacks	99
4.3.2.5	Rare-Earth Oxides Integrated into Germanium MOSFETs	100
4.3.3	Stress and Relaxation of Ge Layer on an Si-Based Substrate	102
4.4	State-of-the-Art Ge CMOS with Recessed Channel and S/D	102
4.4.1	Germanium CMOS Devices	102
4.4.2	Germanium CMOS Circuits	105
4.5	Steep-Slope Device: NCFET	107
4.6	Conclusion	111
	References	112
5	Carbon Nanotube Logic Technology	119
	<i>Jianshi Tang and Shu-Jen Han</i>	
5.1	Introduction – Silicon CMOS Scaling and the Challenges	119
5.2	Fundamentals of Carbon Nanotube	122
5.3	Complementary Logic and Device Scalability Demonstrations	124
5.3.1	CNT NFET and Contact Engineering for CMOS Logic	124
5.3.2	Channel Length Scaling in CNTFET	127
5.3.3	Contact Length Scaling in CNTFET	132
5.4	Perspective of CNT-Based Logic Technology	138
5.4.1	CVD-Grown CNT versus Solution-Processed CNT	138
5.4.2	Purity and Placement of Solution-Processed CNTs	140
5.4.3	Variability in CNTFETs	140
5.4.4	Circuit-Level Integration	142
5.5	Summary and Outlook	142
	References	143
6	Tunnel Field-Effect Transistors	151
	<i>Deblina Sarkar</i>	
6.1	Introduction	151
6.2	Tunnel Field-Effect Transistors: The Fundamentals	153
6.2.1	Working Principle	153

6.2.2	Single-Carrier Tunneling Barrier and Subthreshold Swing	154
6.3	Modeling of TFETs	156
6.4	Design and Fabrication of TFETs	161
6.4.1	Design Considerations	161
6.4.2	Current Status of Fabricated TFETs	162
6.5	Beyond Low-Power Computation	166
6.5.1	Ultrasensitive Biosensor Based on TFET	169
6.5.2	Improvement in Biosensor Response Time	173
	References	175

7 Energy-Efficient Computing with Negative Capacitance 179

Asif I. Khan

7.1	Introduction	179
7.2	How a Negative Capacitance Gate Oxide Leads to Sub-60-Millivolt/Decade Switching	181
7.3	How a Ferroelectric Material Acts as a Negative Capacitor	182
7.4	Direct Measurement of Negative Capacitance in Ferroelectric	186
7.5	Properties of Negative Capacitance FETs: Modeling and Simulation	188
7.6	Experimental Demonstration of Negative Capacitance FETs	190
7.7	Speed of Negative Capacitance Transistors	195
7.8	Conclusions	195
	References	196

8 Spin-Based Devices for Logic, Memory, and Non-Boolean Architectures 201

Supriyo Bandyopadhyay

8.1	Introduction	201
8.2	Spin-Based Devices	203
8.2.1	Spin Field-Effect Transistor (SPINFET)	205
8.2.2	Single Spin Logic Devices and Circuits	209
8.3	Nanomagnetic Devices: A Nanomagnet as a Giant Classical Spin	212
8.3.1	Reading Magnetization States (or Stored Bit Information) in Nanomagnets	215
8.3.2	Writing Magnetization States (or Storing Bit Information) in Nanomagnets	216
8.3.2.1	Spin-Transfer Torque	216
8.3.2.2	Spin-Transfer Torque Aided by Giant Spin Hall Effect	217
8.3.2.3	Voltage-Controlled Magnetic Anisotropy	220
8.3.2.4	Straintronics	224
8.4	Conclusion	231
	Acknowledgments	232
	References	232

9	Terahertz Properties and Applications of GaN	237
	<i>Berardi Sensale-Rodriguez</i>	
9.1	Introduction	237
9.1.1	Applications of Terahertz Technology	237
9.1.2	Terahertz Devices and Challenges	239
9.2	GaN: Properties and Transport Mechanisms Relevant to THz Applications	242
9.2.1	Mobility and Injection Velocity	242
9.2.2	Drift Velocity and Negative Differential Resistance	245
9.2.3	Transport due to Electron Plasma Waves	246
9.3	GaN-based Terahertz Devices: State of the Art	249
9.3.1	High-Electron Mobility Transistors	249
9.3.2	NDR and Resonant Tunneling Devices	252
9.3.3	Quantum Cascade Lasers	254
9.3.4	Electron-Plasma-Wave-based Devices	254
	References	256
	Index	265