

Contents

<i>Temporal Logic Model Checking: Two Techniques for Avoiding the State Explosion Problem</i>	1
Edmund M. Clarke, Jr.	

I. Tools and Computation

<i>Automatic Verification of Extensions of Hardware Descriptions</i>	2
Hans Eveking	

<i>PAPETRI: Environment for the Analysis of Petri Nets</i>	13
G. Berthelot, C. Johnen and Laure Petrucci	

<i>Verifying Temporal Properties of Sequential Machines Without Building their State Diagrams</i>	23
Olivier Coudert, Jean Christophe Madre and Christian Berthet	

<i>Formal Verification of Digital Circuits Using Symbolic Ternary System Models</i>	33
Randal E. Bryant and Carl-Johan Seger	

<i>Vectorized Model Checking for Computation Tree Logic</i>	44
Hiroshi Hiraishi, Shintaro Meki and Kiyoharu Hamaguchi	

<i>Introduction to a Computational Theory and Implementation of Sequential Hardware Equivalence</i>	54
Carl Pixley	

<i>Auto/Autograph</i>	65
Valérie Roy and Robert de Simone	

<i>A Data Path Verifier for Register Transfer Level Using Temporal Logic Language Tokio</i>	76
Hiroshi Nakamura, Yuji Kukimoto, Masahiro Fujita and Hidehiko Tanaka	

<i>The Use of Model Checking in ATPG for Sequential Circuits</i>	86
Paolo Camurati, M. Gilli, P. Prinetto and M. Sonza Reorda	

<i>Compositional Design and Verification of Communication Protocols, Using Labelled Petri Nets</i>	96
Jean Christophe Lloret, Pierre Azéma and François Vernadat	

<i>Issues Arising in the Analysis of L.O.</i>	106
Linda Ness	

<i>Automated RTL Verification Based on Predicate Calculus</i>	116
Michel Langevin	

<i>On Using Protean To Verify ISO FTAM Protocol</i>	126
Richard Lai, Ken R. Parker and T. S. Dillon	
<i>Quantitative Temporal Reasoning</i>	136
E. Allen Emerson, A. K. Mok, A. Prasad Sistla and Jai Srinivasan	
II. Partial Orders	
<i>Using Partial-Order Semantics to Avoid the State Explosion Problem in Asynchronous Systems</i>	146
David K. Probst and Hon F. Li	
<i>A Stubborn Attack On State Explosion</i>	156
Antti Valmari	
<i>Using Optimal Simulations to Reduce Reachability Graphs</i>	166
Ryszard Janicki and Maciej Koutny	
<i>Using Partial Orders to Improve Automatic Verification Methods</i>	176
Patrice Godefroid	
III. Reduction in Finite State Systems	
<i>Compositional Minimization of Finite State Systems</i>	186
Susanne Graf and Bernhard Steffen	
<i>Minimal Model Generation</i>	197
A. Bouajjani, Jean-Claude Fernandez and Nicholas Halbwachs	
<i>A Context Dependent Equivalence Relation Between Kripke Structures</i>	204
Bernhard Josko	
<i>The Modular Framework of Computer-Aided Verification</i>	214
Gil Shurek and Orna Grumberg	
IV. Automaton Models	
<i>Verifying Liveness Properties by Verifying Safety Properties</i>	224
Jerry R. Burch	
<i>Memory Efficient Algorithms for the Verification of Temporal Properties</i>	233
Costas Courcoubetis, Moshe Vardi, Pierre Wolper and Mihalis Yannakakis	
<i>A Unified Approach to the Deadlock Detection Problem in Networks of Communicating Finite State Machines</i>	243
Wuxu Peng and S. Purushothaman	
<i>Branching Time Regular Temporal Logic for Model Checking with Linear Time Complexity</i>	253
Kiyoharu Hamaguchi, Hiromi Hiraishi and Shuzo Yajima	

<i>The Algebraic Feedback Product of Automata</i>	263
Victor Yodaiken	
V. Model Synthesis	
<i>Synthesizing Processes and Schedulers from Temporal Specifications</i>	272
Howard Wong-Toi and David L. Dill	
<i>Task-Driven Supervisory Control of Discrete Event Systems</i>	282
Christian H. Golaszewski and Robert P. Kurshan	
<i>A Proof Lattice-Based Technique for Analyzing Liveness of Resource Controllers</i>	292
Ugo Buy and Robert Moll	
VI. Theorem-Provers	
<i>Verification of a Multiprocessor Cache Protocol Using Simulation Relations and Higher-Order Logic</i>	302
Paul Loewenstein and David L. Dill	
<i>Computer Assistance for Program Refinement</i>	312
David A. Carrington and K. A. Robinson	
<i>Program Verification by Symbolic Execution of Hyperfinite Ideal Machines</i>	322
James M. Morris and Mark Howard	
VII. Process Algebra	
<i>Extension of the Karp and Miller Procedure to Lotos Specifications</i>	333
Michel Barbeau and Gregor V. Bochmann	
<i>An Algebra for Delay-Insensitive Circuits</i>	343
Mark B. Josephs and Jan Tijmen Udding	
<i>Finiteness Conditions and Structural Construction of Automata for All Process Algebras</i>	353
Eric Madelaine and Didier Vergamini	
<i>On Automatically Explaining Bisimulation Inequivalence</i>	364
Rance Cleaveland	