

Table of Contents

Session 1: Fault-Tolerance Techniques	1
<i>Chair: Winfried Görke, University of Karlsruhe, Germany</i>	
A Model for Adaptive Fault-Tolerant Systems	3
<i>M. A. Hiltunen, R. D. Schlichting (University of Arizona, Tucson, USA)</i>	
Designing Secure and Reliable Applications using Fragmentation- Redundancy-Scattering: An Object-Oriented Approach.....	21
<i>J.-C. Fabre, Y. Deswartes (LAAS-CNRS, Toulouse, France), B. Randell (University of Newcastle-upon-Tyne, United Kingdom)</i>	
A Fault-Tolerant Mechanism for Simple Controllers	39
<i>J. G. Silva, L. M. Silva, H. Madeira, J. Bernardino (University of Coimbra, Portugal)</i>	
 Session 2: Formal Methods	 57
<i>Chair: John McDermit, University of York, United Kingdom</i>	
Formal Semantics for Ward & Mellor's Transformation Schemas and the Specification of Fault-Tolerant Systems.....	59
<i>C. Petersohn, W.-P. de Roeper (Christian-Albrechts-University of Kiel, Germany), C. Huizing (Eindhoven University of Technology, The Netherlands), J. Peleska (DST GmbH, Kiel, Germany)</i>	
Formal Reasoning on Fault Coverage of Fault Tolerant Techniques: a Case Study	77
<i>C. Bernardeschi, A. Fantechi, L. Simoncini (University of Pisa, Italy)</i>	
 Session 3: Evaluation	 95
<i>Chair: Bjarne Helvik, DELAB, Trondheim, Norway</i>	
On Performability Modeling and Evaluation of Software Fault Tolerance Structures.....	97
<i>S. Chiaradonna, A. Bondavalli (CNUCE/CNR, Pisa, Italy), L. Strigini (IEI/CNR, Pisa, Italy)</i>	
Optimal Design of Fault-Tolerant Soft-Real-Time Systems with Imprecise Computations.....	115
<i>C. Antonelli (Tor Vergata University of Rome, Italy), V. Grassi (University of Perugia, Italy)</i>	

Computational Restrictions for SPN with Generally Distributed Transition Times.....	131
<i>A. Bobbio (University of Brescia, Italy), M. Telek (Technical University of Budapest, Hungary)</i>	
Session 4: Hardware Testing	149
<i>Chair: Bernd Straube, Fraunhofer – EAS, Dresden, Germany</i>	
Test Generation for Digital Systems Based on Alternative Graphs	151
<i>R. Ubar (Technical University of Tallinn, Estonia)</i>	
The Configuration Ratio: A Model for Simulating CMOS Intra-Gate Bridge with Variable Logic Thresholds.....	165
<i>M. Renovell, P. Huc, Y. Bertrand (University of Montpellier II, France)</i>	
Coverage of Delay Faults: When 13% and 99% Mean the Same	178
<i>A. Krásniewski, L. B. Wroński (Warsaw University of Technology, Poland)</i>	
Session 5: Fault Injection	197
<i>Chair: Jean Arlat, LAAS-CNRS, Toulouse, France</i>	
RIFLE: A General Purpose Pin-level Fault Injector.....	199
<i>H. Madeira, M. Rela, F. Moreira, J. G. Silva (University of Coimbra, Portugal)</i>	
On Single Event Upset Error Manifestation.....	217
<i>R. Johansson (Chalmers University of Technology, Göteborg, Sweden)</i>	
Session 6: Software Testing	233
<i>Chair: Pierre-Jacques Courtois, AIB-Vincotte Nuclear, Brussels, Belgium</i>	
Injecting Faults into Environment Simulators for Testing Safety Critical Software.....	235
<i>H. Zhu, P. A. V. Hall, J. H. R. May (The Open University, Milton Keynes, United Kingdom), T. Cockram (Rolls Royce plc., United Kingdom)</i>	
On Statistical Structural Testing of Synchronous Data Flow Programs.....	250
<i>P. Thévenod-Fosse, C. Mazuet, Y. Crouzet (LAAS-CNRS, Toulouse, France)</i>	
Session 7: Built-In Self Test	269
<i>Chair: Andrzej Hlawiczka, Technical University of Gliwice, Poland</i>	
Hierarchical Test Analysis of VLSI Circuits for Random BIST	271
<i>G. Masseboeuf (Laboratoire d'Automatique de Grenoble, France), J. Pulou, J. L. Rainard (CNET, Meylan, France)</i>	
Zero Aliasing Compression Based on Groups of Weakly Independent Outputs in Circuits with High Complexity for Two Fault Models.....	289
<i>P. Böhlau (University of Potsdam, Germany)</i>	

Session 8: Software Diversity	307
<i>Chair: Hubert Kirrmann, ASEA Brown Boveri AG, Baden-Dätwil, Switzerland</i>	
Systematic and Design Diversity – Software Techniques for Hardware Fault Detection.....	309
<i>T. Lovric (University of Dortmund, Germany)</i>	
Detection of Permanent Hardware Faults of a Floating Point Adder by Pseudoduplication.....	327
<i>S. Gerber, M. Gössel (University of Potsdam, Germany)</i>	
MLDD (Multi-Layered Design Diversity) Architecture for Achieving High Design Fault Tolerance Capabilities.....	336
<i>A. Watanabe, K. Sakamura (University of Tokyo, Japan)</i>	
 Session 9: Parallel Systems	 351
<i>Chair: Paulo Veríssimo, INESC, Lisbon, Portugal</i>	
Reconfiguration and Checkpointing in Massively Parallel Systems.....	353
<i>B. Bieker, E. Maehle (University of Paderborn, Germany), G. Deconinck, J. Vounckx (Catholic University of Leuven, Belgium)</i>	
An Approach for Hierarchical System Level Diagnosis of Massively Parallel Computers Combined with a Simulation-Based Method for Dependability Analysis.....	371
<i>J. Altmann, F. Balbach, A. Hein (University of Erlangen-Nürnberg, Germany)</i>	
Hierarchical Checking of Multiprocessors Using Watchdog Processors.....	386
<i>I. Majzik, A. Pataricza (Technical University of Budapest, Hungary), M. Dal Cin, W. Hohl, J. Hönig, V. Sieh (University of Erlangen-Nürnberg, Germany)</i>	
 Panel Discussion: Future Directions in Dependable Computing	 405
<i>Moderator: Jean-Claude Laprie, LAAS-CNRS, Toulouse, France</i>	
Dependability: The Challenge for the Future of Computing and Communication Technologies.....	407
<i>J.-C. Laprie (LAAS-CNRS, Toulouse, France)</i>	
Position Paper.....	409
<i>A. Avizienis (University of California, Los Angeles, USA)</i>	
Position Paper.....	411
<i>J. Hlavicka (Czech Technical University, Prague, Czech Republic)</i>	
Position Paper.....	412
<i>M. Morganti (ITALTEL Central Research Labs, Milano, Italy)</i>	

Some Lessons from the SW2000 Workshop.....	414
<i>B. Randell (University of Newcastle-upon-Tyne, United Kingdom)</i>	
Dependable Computing and its Industrial Use.....	417
<i>E. Schmitter (Siemens AG, Munich, Germany)</i>	
Session 10: Fault Tolerance in VLSI	419
<i>Chair: József Sziray, Computer Research and Innovation Center, Budapest, Hungary</i>	
An Effective Reconfiguration Process for Fault-Tolerant VLSI/WSI Array Processors.....	421
<i>Y.-Y. Chen, C.-H. Cheng, Y.-C. Chou (Chung-Hua Polytechnic Institute Hsin-Chu, Taiwan)</i>	
Concurrent Error Detection in Fast FNT Networks	439
<i>J. M. Tahir, S. S. Dlay, R. N. Gorgui-Naguib, O. R. Hinton (University of Newcastle-upon-Tyne, United Kingdom)</i>	
Feasible Regions Quantify the Configuration Power of Arrays with Multiple Fault Types.....	453
<i>L. E. LaForge (University of Nevada, Reno, USA)</i>	
Session 11: Measurement	471
<i>Chair: Taschko Nikolov, Technical University of Sofia, Bulgaria</i>	
Software Reliability Analysis of Three Successive Generations of a Switching System.....	473
<i>M. Kaàniche, K. Kanoun, M. Cukier (LAAS-CNRS, Toulouse, France), M. Bastos Martini (CpQD-Telebras, Brazil)</i>	
Performance of Consistent Checkpointing in a Modular Operating System: Results of the FTM Experiment	491
<i>G. Muller (IRISA/INRIA, Rennes, France), M. Hue, N. Peyrouze (Bull Research, France)</i>	
Session 12: Switching Networks and Hypercubes	509
<i>Chair: K. Iyoudou, Moscow Aviation Institute, Russia</i>	
Ring-Banyan Network: A Fault Tolerant Multistage Interconnection Network and its Fault Diagnosis	511
<i>J.-H. Park, H.-K. Lee (Korea Advanced Institute of Science and Techno- logy, Taejon, Korea), J.-H. Cho (Electronics and Telecommunications Research Institute, Taejon, Korea)</i>	
Reconfiguration of Faulty Hypercubes	529
<i>D. R. Avresky, K. M. Al-Tawil (Texas A&M University, College Station, Texas)</i>	

Fault-Tolerance on Boolean n-Cube Architectures	546
<i>C.-S. Yang (National Sun Yat-Sen University, Kaohsiung, Taiwan),</i>	
<i>S.-Y. Wu (Chinese Military Academy, Kaohsiung, Taiwan)</i>	
Session 13: Distributed Systems	561
<i>Chair: Jan Torin, Chalmers University of Technology, Göteborg, Sweden</i>	
Relative Signatures for Fault Tolerance and their Implementation.....	563
<i>M. Leu (University of Dortmund, Germany)</i>	
GATOSTAR: A Fault Tolerant Load Sharing Facility for Parallel Applications.....	581
<i>B. Folliot, P. Sens (MASI Laboratory, Paris, France)</i>	
A Hierarchical Membership Protocol for Synchronous Distributed Systems.....	599
<i>P. D. V. van der Stok, M. M. M. P. J. Claessen, D. Alstein</i>	
<i>(Eindhoven University of Technology, The Netherlands)</i>	
Author Index	617