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2D Electronic Circuits for Sensing Applications

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1.1 Introduction

Technology has always been around, be it the most straightforward wooden wheel or a more complex system like a modern car. Technology's and science's evolution pave the way for society's evolution. One of the most relevant breakthroughs in the past years was the transistor's discovery in 1947. This discovery allowed for replacing the vacuum tube, also known as the valve, with a device with a smaller footprint and higher efficiency. This discovery led to a massive bump in industrial society's evolution. Technology fully integrates people's lives, either directly in the devices they use (e.g. smartphones) or indirectly through those who provide them with a service (e.g. mobile operators' signal coverage).

This revolution was possible due to the miniaturization of the electronic components that integrate transistors while maintaining or improving their performance. According to Moore's Law, the number of transistors in the same chip area doubles every two years. This law has been confirmed for over 50 years, but it is getting to a point where reducing component size is reaching its physical limitations due to short-channel effects and interconnect's heating [1, 2]. Further research on new materials is required to replace silicon before a new paradigm in nanoelectronics – more than Moore – can be reached.

In recent years, two-dimensional (2D) materials have become the focus of many investigations to replace silicon to continue downscaling electronic devices [3–6]. Many of these materials show excellent electronic, photoelectronic, and mechanical properties. Therefore, investigating the implementation of a technology based on

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such materials is increasingly important as the Internet of Things (IoTs) becomes more prevalent and requires a massive number of devices with a small footprint to be integrated without much notice. Although these are promising materials, their integration with standard manufacturing processes and replicability outside of the laboratory is yet to be achieved [7]. Many other problems associated with interfacing 2D and other materials continue to be challenging since these interfaces usually degrade their electronic properties, especially the carrier mobility, reducing their overall performance [8, 9].

The first 2D material discovered was graphene by Andre Geim and Konstantin Novoselov in 2004, which led them to win the Nobel Prize in Physics in 2010 [10]. The graphene was obtained using tape to exfoliate graphite until it reached a single atomic layer. The discovery of graphene launched curiosity and investigations toward graphene and other 2D materials. These days, the investigation of 2D materials has progressed immensely, to the point where we can already separate 2D materials into families according to their elements' chemical composition, unit cell, electronic, optical, or structural properties [11]. The most known families are X-enes and transition-metal dichalcogenides (TMDs). X-enes group single element materials with atoms organized in a hexagonal lattice, which is the case of graphene, silicene, germanene, and others. TMDs group 2D materials of the form MX_2, where M is a transition metal from the 4th, 5th or 6th group, and X is a chalcogen from group 16th. The most known TMDs are molybdenum disulfide, tungsten disulfide, and molybdenum diselenide. Since some 2D materials were discovered recently, their science and technology are not sufficiently mature to place them as candidates for next-generation electronic materials. Therefore, limit our discussion to graphene and MoS_2 since, as of today, they are by far the most studied materials.

Graphene consists of a single graphite layer of carbon atoms arranged in a hexagonal lattice. Graphene can be grown at a large scale by chemical vapor deposition (CVD) [12, 13] or liquid-phase exfoliation (LPE). One of the problems with graphene fabrication is that it cannot be grown directly on most substrates. It is usually deposited on a transition metal catalyst foil – often copper or nickel – and then transferred using a wet or dry transfer process to the desired substrate [14]. Because of the need to transfer to the final substrate, graphene's performance is affected by the degradation of its carrier mobility during this transfer process [15]. Graphene has remarkable properties, such as extremely high carrier mobility ($2000\,cm^2\,V^{-1}\,s^{-1}$ for any mechanically transferred graphene [16] and $200\,000\,cm^2\,V^{-1}\,s^{-1}$ for suspended graphene [17]) when compared to silicon ($1400\,cm^2\,V^{-1}\,s^{-1}$ for electrons and $450\,cm^2\,V^{-1}\,s^{-1}$ for holes), good electrical conductivity ($\approx 10^4\,\Omega^{-1}\,cm^{-1}$ [17]), high thermal conductivity ($5300\,Wm^{-1}\,K^{-1}$ [18]), and high Young's modulus (0.5–1.0 TPa [16]). This material is a gapless semiconductor, meaning it has a 0 eV energy gap. Because of this intrinsic property, this material cannot be used in devices where the off state is needed since the material always conducts electricity by holes or electrons. These properties make graphene a possible solution to overcome silicon limitations in certain applications and can be implemented in devices with a broad range of uses, from high-speed electronics to sensing applications.

MoS_2 belongs to the TMDs family and consists of a molybdenum layer sandwiched between two sulfur layers. This material appears in nature as molybdenite, and, like graphene, can be fabricated using CVD or exfoliation techniques. Unlike graphene, MoS_2 properties are not all well-defined, but its carrier mobility has been shown to have values up to 200 $cm^2\ V^{-1}\ s^{-1}$ at room temperature and Young's modulus of 0.33 TPa [19]. Different from graphene, MoS_2 has a direct bandgap of 1.8 eV [20], which means it can be used in devices that need to have an off state.

Due to the remarkable properties of these materials, their implementation on capacitors, inductors, and field-effect transistors (FETs) has already been reported in numerous papers. In Sections 1.2, 1.3, and 1.4, the literature on these components will be explored, regarding their physical implementation and the models that try to predict these components' behavior.

1.2 Graphene Inductors

On-chip inductors revolutionized RF electronics in the 1990s, but not everything is excellent. These inductors are planar and must have a large area, as dictated by electromagnetic laws, which means they cannot be downsized alongside standard transistors while maintaining high inductance density. In some cases, it is reported that planar inductors occupy up to 50% of an integrated circuit area. Thus, they hinder further miniaturization and integration. Finding new approaches to making these devices is imperative.

It is well known that the inductance is shape- and size-dependent, but in graphene a third factor can be explored, known as *kinetic inductance*. This material property arises from the inertia of charge carriers moving in alternating electric fields. Like all mass particles, charge carriers preserve their momentum, so when in an alternating electric field, it takes a finite time to change their momentum according to the field, which manifests as kinetic inductance. It is not very important in conventional metals because their conductance is associated with higher carrier concentration and macroscopic thickness. The kinetic inductance manifests as an equivalent series inductance, adding to the geometric inductance associated with the shape/size. Therefore, materials with high kinetic inductance must be used to reduce inductor size while maintaining high inductance density. Graphene is being exploited as a possible solution to the inductance component miniaturization issue due to its atomic thickness and relatively high conductivity, based on high carrier mobility and low carrier concentration. Consequently, graphene has high kinetic inductance and a small footprint.

A multilayer graphene (MLG) inductor is proposed in [21], shown in Figure 1.1. The authors' choice of using MLG is to ensure a lower quantum contact resistance (resistance associated with the interface between graphene and metal contact). This approach raises two problems: when compared with metals, graphene has a much lower conductivity; compared to SLG, the MLG exhibits reduced charge carrier inertia due to interlayer coupling. Bromine intercalation is used to overcome these

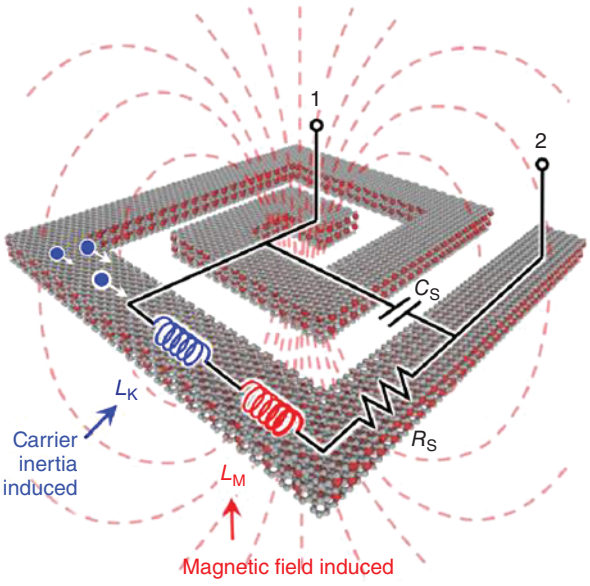

Figure 1.1 Schematic of a spiral inductor and its simplified equivalent circuit. L_M and L_K are the magnetic and kinetic inductance, respectively. R_S and C_S are the series resistance and the inter-turn capacitance, respectively. Source: Reproduced with permission from Kang et al. [21]/Springer Nature.

issues by increasing conductivity and reducing interlayer coupling. When compared to copper inductors, this method can achieve Q-factors of up to 12, and 1.5-times higher inductance in a two-turn inductor when compared to copper ones. The authors also claim that it is possible to achieve better results by improving intercalation technology and increasing contact quality.

1.2.1 Modeling of Graphene Inductors

The modeling of graphene inductors is not perfectly established, and most works are based on extracting parameters from or simulating typical metallic structures, adding some parameters to better match graphene characteristics.

In [21], the authors affirm that current simulation tools cannot capture the physics of graphene in modeling impedance/inductance. To try and predict the inductor behavior, the authors start by analyzing the performance of the inductors through finite element method (FEM) simulations in ANSYS HFSS and then modeled bulk coils with electrical conductivities considering grain boundary and surface scattering effects at the micro- and nanoscale for metals, and graphene conductivities extracted from DC analysis.

Although modeling graphene inductors remains a challenge, a simple model of a graphene spiral inductor can be seen in Figure 1.2. In this model, it can be corroborated that L_k appears in series with L_M, the substrate and dielectric need to be considered, and an inter-turn coupling capacitance appears, resulting from the inductor

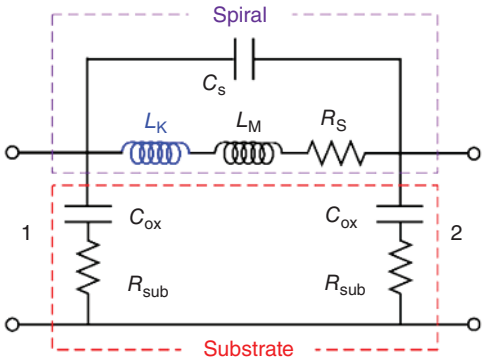

Figure 1.2 Simplified circuit model for a two-turn inductor. L_K, L_M, and R_S are the kinetic inductance, magnetic inductance, and series resistance of graphene inductor, respectively. C_s is the inter-turn coupling capacitance. C_{ox} and R_{sub} are substrate dielectric capacitance and substrate resistance, respectively. Source: Adapted from [21].

design. This model predicts that the substrate and the inter-turn coupling degrade the inductor's behavior at higher frequencies.

By using Launder's approach, the kinetic inductance per unit length is given by:

$$L_k = \frac{2\pi\hbar}{e^2 v_F M} \approx \frac{81\,\text{nH}}{M}/\,\mu\text{m} \tag{1.1}$$

where M is the number of quantum modes $\left(M = \frac{\Delta E_F}{\pi\hbar v_F}\right)$, ΔE_F is the difference between Dirac point energies and Fermi level, W is the width of graphene, e is the electron charge, $\hbar$ is the reduced Planck's constant, and v_F is the Fermi velocity.

The figure of merit (FOM) of an inductor is the quality factor (Q-factor) and is expressed as follows:

$$Q_{\text{factor}} = -\frac{\text{Imag}\left(Y_{12}\right)}{\text{Real}\left(Y_{12}\right)} = \frac{Z_L}{R} = \frac{wL}{R} \tag{1.2}$$

where Y_{12} is an admittance parameter $\left(Y_{12} = -\frac{2S_{12}}{\left(1+S_{11}\right)\left(1+S_{22}\right)-S_{12}S_{21}}\right)$, L and R are the inductance and resistance of the inductor, and w is the angular frequency.

1.3 Graphene Capacitors

A capacitor is a passive device that stores electrical energy and adds capacitance to a circuit. The main usages of this device are to serve as a signal filter, for example, in a ladder design or as a temporary battery. The simplest capacitor consists of two parallel metal plates separated by a dielectric material, and the energy stored

depends on the area of the plates, the distance between plates, the permittivity, and the dielectric function. Capacitors based on 2D materials have been explored, and the most common material used is graphene. Most of the work is done in biosensing, but research in the RF branch is emerging.

Graphene is used in the biosensing scene due to the possibility of functionalizing the graphene's surface. By immobilizing molecular probes on graphene using a linker, it is possible to change the graphene's surface charge density whenever there is a biorecognition event. This change in accumulation or depletion happens due to the charged or polar target molecules' local gating, which modulates the graphene channel conductance. The effect is capacitive, where the capacitance is that of the electrical double layer (EDL) forming at the graphene-solution interface. Consequently, different target molecule concentrations induce different amounts of charge in the EDL capacitor, which will be mirrored on the opposite plate of the capacitor, i.e the graphene surface.

There are no well-defined characteristics of graphene capacitors on the RF branch, but due to the high quantum capacitance and tuning possibility, some works claim that graphene is an excellent candidate. Moreover, the small footprint and low control voltage allow the development of compact systems like voltage-controlled oscillators, tunable filters, and phase shifters.

In [22], a variable capacitor based on graphene was implemented as a glucose sensor. This device takes advantage of the carrier density change in functionalized graphene when the adsorbed molecules' concentration changes, leading to the modulation of the channel conductance. As shown in Figure 1.3, aside from the capacitance dependence on adsorbed molecule concentration, it also depends on the gate voltage and ranges from 90 to 140 pF.

Another capacitor with tunable control based on graphene was studied for RF applications, with capacitance between 3.8 and 2.9 pF, a gate voltage of 1.25 V, and frequencies ranging from 1 to 10 GHz [23]. The best device performance was achieved with 1.25 V gate voltage and 0.4 GHz frequency, obtaining a Q-factor of up

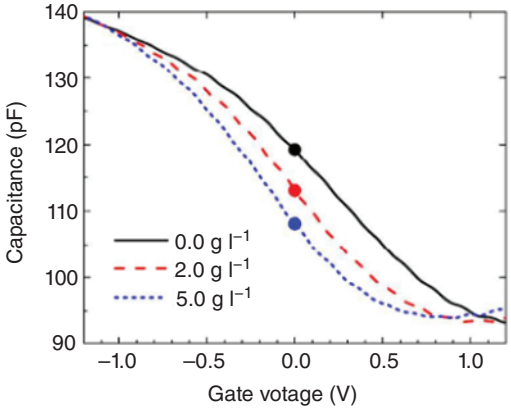

Figure 1.3 Capacitance-voltage curves. Source: Reproduced with permission from Zhang et al. [22]/American Chemical Society.

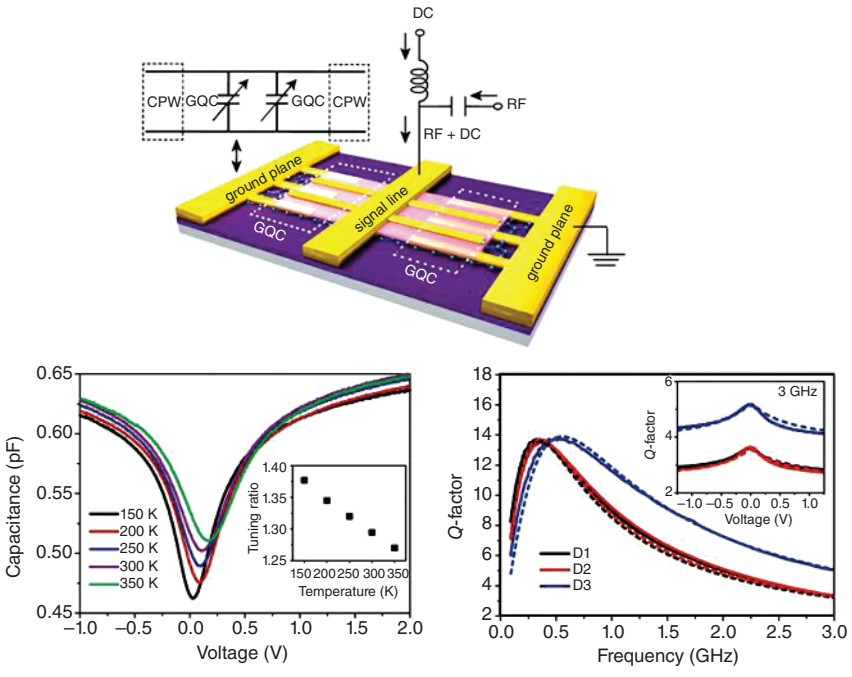

Figure 1.4 Schematic of the graphene quantum capacitor (left), capacitance dependence on frequency and DC bias (center) and *Q*-factor dependence on frequency (right). Source: Reproduced with permission from Moldovan et al. [23]/American Chemical Society.

to 14.5. The device consists of two symmetrically placed capacitors in a parallel configuration so that they can be characterized at microwave frequencies. This design also uses a multi-finger approach to increase the capacitance while reducing graphene's parasitic resistance. From Figure 1.4, it is possible to see that by changing the DC bias, the capacitance also changes, allowing for low-power ICs. With this design, the maximum *Q*-factor obtained is 15 at 0.4 GHz, but the authors say it is possible to increase it with simple design changes.

In [24], the same authors explored the design described above. By changing the fingers' number and size, the authors concluded the *Q*-factor increases when reducing the finger length and that the number of fingers does not have much impact on the *Q*-factor. It was also concluded that changing the number of fingers makes it possible to scale the capacitors to any capacitance while maintaining similar *Q*-factors. The best device achieved a *Q*-factor of 12 at 1 GHz, an improvement from the first study, where at 1 GHz the *Q*-factor was about 9.

Another tunable graphene capacitor is explored in [25]. This design (Figure 1.5) is more straightforward than the previous one discussed and consists of a parallel capacitor where the bottom plate is graphene, the dielectric is hexagonal boron nitride (hBN), and the top plate is chromium (Cr) and gold (Au). From the graph, it can be proved that the capacitor is tunable and that it has a minimum capacitance of around 3.5 pF.

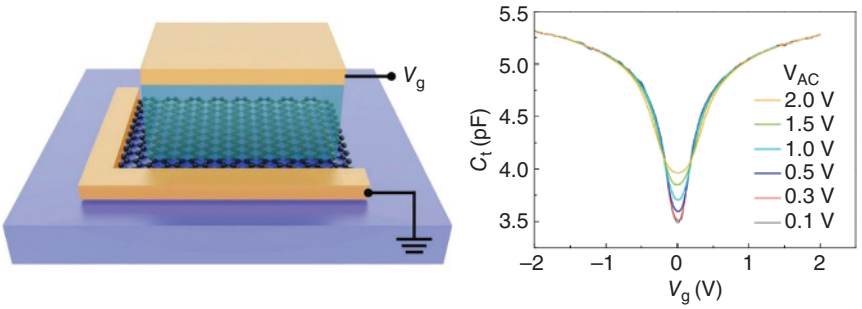

Figure 1.5 Schematic of graphene tunable capacitor (left) and capacitance dependence on bias voltage and AC signal voltage (right). Source: Reproduced with permission from Zhang et al. [25]/John Wiley & Sons.

1.3.1 Modeling Graphene Capacitors

As for graphene inductors, state-of-the-art in graphene capacitor modeling is not well established, and due to the differences between designs, the models available may not suit all designs.

In [24], the authors used the circuit model in Figure 1.6 to extract the device parameters for the proposed design. In this model, a series resistance ($R_C + R_M + R_{GS}$) is observed along with an oxide capacitance (C_{ox}) that raises from the material's intrinsic properties. The graphene layer raises variable resistance (R_G) and quantum capacitance C_q. The quantum capacitance of graphene is reported as:

$$C_q = \frac{2e^2 k_B T}{\pi(\hbar v_F)^2} \ln\left[2\left(1+\cosh\left(\frac{eV_{ch}}{k_B T}\right)\right)\right] LWN \tag{1.3}$$

where e is the electron charge, k_B is the Boltzmann's constant, T is the temperature, $\hbar$ is the reduced Plank's constant, v_F is the Fermi velocity, V_{ch} is the graphene potential, N is the number of fingers, and L and W are the length and width of the fingers.

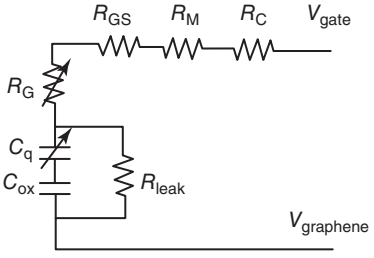

Figure 1.6 Circuit model used to extract the device parameters. R_C is the contact resistance. R_M is the metal fingers resistance. R_{GS} is the graphene resistance in the interspace. R_G is the graphene resistance. C_q is the graphene quantum capacitance. C_{ox} is the fixed oxide capacitance. Source: Reproduced with permission from Moldovan et al. [24]/American Chemical Society.

For a more straightforward design [25], the authors propose an equivalent circuit composed of two capacitors in series. One is the geometrical capacitance which depends on the hBN thickness and dielectric constant and is defined as $C_{\text{is}} = \frac{\varepsilon}{t_{\text{hBN}}}$. The other is the quantum capacitance of the graphene and is defined as $C_{\text{q}} = \text{d}Q/\text{d}V_{\text{ch}}$, where Q is the charge induced on the graphene and V_{ch} the graphene potential. Far from the Dirac point, C_{q} is much larger than C_{is}. So, in that region, the quantum capacitance can be neglected, but it must be considered when close to the Dirac point.

Similar to the inductors, the FOM of a capacitor is the Q-factor and is expressed as:

$$Q_{\text{factor}} = -\frac{\text{Imag}\left(Y_{12}\right)}{\text{Real}\left(Y_{12}\right)} = \frac{Z_C}{R} = \frac{1}{wCR} \tag{1.4}$$

where Y_{21} is an admittance parameter, C and R are the capacitance and resistance of the inductor, and w is the angular frequency.

1.4 2D Material Transistors

Transistors are one of the essential components of modern electronics and can be found in almost every electronic system, to amplify or switch electrical signals. There are several types of transistors, the most relevant for micro- and nanoelectronics being the FET. These devices are based on channel conductance modulation by applying a voltage to the gate. It means we can control the current that flows between the drain and source terminals, I_{DS}, using a gate voltage applied to a third contact, which is electrically insulated from the other two. The gate contact and the FET channel coupling are capacitive and have been discussed to some extent in Section 1.3.

The most important part of the transistor is the channel, which forms in the semiconductor material at the interface with the gate dielectric. Most common chips use transistors with silicon channels and rely on reducing the channel's size to improve their overall performance. In simple terms, reducing transistor size allows for more integration in the same chip's area, increasing the chip performance and speed. However, due to short-channel effects and transistor Cu interconnects heating due to increased speed; their downscaling is becoming a considerable challenge. To overcome this issue and ensure technological advancement, further research on new materials to replace silicon must be undertaken. As a result of the effort to find new materials to replace silicon, 2D materials appeared as a possible solution because of their high saturation velocity and high carrier mobility, being the most promising graphene and MoS_2.

These materials can be used in transistors for RF applications, such as oscillators, frequency multipliers, transceivers, or mixers.

1.4.1 Most Common Topologies for Transistors

The common topologies of graphene field-effect transistors (GFETs) are those found in other technologies, namely top-gated, back-gated, and top/back-gated GFETs, Figure 1.7. What gives the name to these topologies is the position of the gate. Although the difference between these topologies may look simple, changing the position of the gate has implications on the fabrication methodology, expected performance, modeling considerations, and applications.

Top-gated GFETs are reported in the literature with their implementation in RF applications, biosensors, and liquid-gate GFETs. This approach is excellent when it is necessary to have greater control over the channel modulation while using lower gate bias by using a thin gate oxide layer. The major problem with this topology is the need to grow an oxide layer on top of the graphene without damaging its structure and consequently degrading its carrier mobility. To overcome this issue, researchers are trying new approaches, such as the physical transfer of a nanowire to function as a gate electrode or the use of boron nitride (h-BN), or the refinement of standard fabrication techniques like atomic layer deposition (ALD) or thermal growth.

Back-gated structures expose the channel, allowing the graphene's surface to interact with light or molecules. Both interactions produce changes in graphene's properties and, therefore, changes in the transfer characteristic, allowing the evaluation of the element that caused the change. This behavior makes back-gated GFETs suitable for biosensors and photodetectors. The major problem with this approach is the necessity of high voltage to control the device, which is a drawback for most common applications.

Top/back-gated structures are used when it is advantageous to split the DC and AC parts of the gate voltage and apply them to different contacts. In this way, a constant quiescent bias can be applied to the back gate – setting the transistor functioning point – while a signal is applied to the top gate in this case, modulating the transfer characteristics around the GFET quiescent point. Since GFETs' technology is still early, researchers use this topology to tune all their devices equally. Another

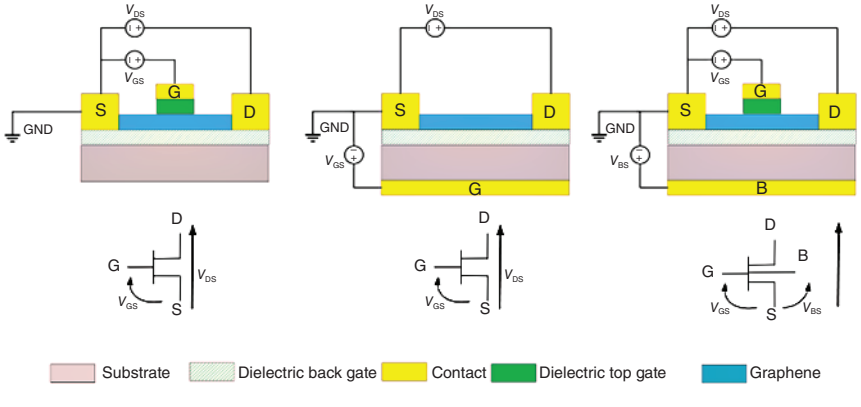

Figure 1.7 Top-gated (left), back-gated (center) and top/back-gated (right) graphene transistors. Source: Jmai et al. [26]/MDPI/CC BY 4.0.

architecture reported in [27] uses receded gate geometry. It is adequate for liquid-gate transistors working as chemical sensors since, like in the bottom gate case; it leaves the channel accessible for the molecules in the solution. Moreover, it uses the EDLs formed at the solid–liquid interfaces as the gate dielectric, providing a supercapacitor that allows operation at very low voltage, which is critical when dealing with biomolecules, cells, and microorganisms.

Graphene transistors (GFETs) have some unique characteristics. The first is that they cannot be turned off. Conventional transistors have a threshold gate voltage below which no current flows between drain and source and they are turned off. This property allows conventional transistors to be used in digital systems. On the contrary, GFETs do not have a minimum gate voltage to turn on; they have a specific voltage at which they exhibit the minimum I_{DS}, which is called the Dirac voltage. The second unique property of GFETs is their ambipolar character. Whereas, for example, silicon FETs are either n- or p-type, but not both simultaneously, because their doping is achieved by impurity doping, which acts as donors (n-doping) or acceptors (p-doping), but not both, GFETs can be seen as p- and n-type transistors in the same device, whereby adjusting the gate voltage to the left or right of the Dirac voltage switches from p- to n-type transistors. Although this is an obstacle for digital applications, it is possible to implement them in analog systems. These analog systems can be biosensors, flexible electronics, or radiofrequency circuits. The third unique property of GFETs stems from graphene's very high carrier mobility, which is essential for developing transistors with high cut-off (f_T) frequencies or biosensors with exceedingly high sensitivity. GFETs with $f_T = 100$ GHz were reported in [28], and many others and the purpose of their investigation can be seen in Table 1.1. GFETs found in the literature are not easy to replicate, so further research is still needed to integrate these devices into a system.

Unlike GFETs, MoS_2 transistors (MoS_2 FETs) work like conventional FETs; they can be turned off. Therefore, MoS_2 FETs can be used in digital systems, which makes them a possible replacement for silicon-based transistors. MoS_2 single-layer FETs with f_T of 6.7 GHz and f_{max} of 5.3 GHz were reported in [44]. Although the design frequencies and the carrier mobility in MoS_2 are lower than those in graphene, the presence of a bandgap enables more significant voltage gain compared to GFETs. In another publication, by using a few-layer MoS_2, it was achieved a f_T of 42 GHz and f_{max} of 50 GHz [20]. Although MoS_2 FETs may look great, the low mobility of MoS_2 can be a limitation for their application in the higher frequency domain. The lack of models makes it difficult to predict the behavior of these devices, and the state-of-the-art of such devices is still too poor compared to graphene FETs. Further research is needed to understand the true potential of these devices.

1.4.2 Modeling of 2D Materials-Based Transistors

Simulating a device's performance is a key success factor of modern electronics, and because of that, modeling GFETs plays an important role in helping researchers achieve GFETs' best performance and understanding if their implementation in more complex devices is reliable, allowing for the substitution of silicon transistors.

Table 1.1 Graphene FETs found in the literature.

	Purpose	Graphene type	Differentiating approach	Performance	References
Top gated	Achieve high transconductance and drain-current saturation	CVD	Self-aligned source/drain electrodes	Maximum $g_m = 250\ \mu S\ \mu m^{-1}$	[29]
	RF applications	Mechanical exfoliation	Nanowire as the gate and self-aligned source/drain	Maximum $g_m = 1.27\ mS\ \mu m^{-1}$ and intrinsic $f_T = 300$ GHz	[30]
	Improve the drain-current saturation	CVD	Thin Al_2O_3 gate oxide dielectric (~4 nm)	$\frac{f_{max}}{f_T} > 3$ $A_v > 30$ dB	[31]
	RF applications	Mechanical exfoliation	Dual top gate	Maximum $g_m = 550\ \mu S\ \mu m^{-1}$ and intrinsic $f_T = 14.7$ GHz	[32]
	RF applications	CVD	T-shaped gate and drain/source	Intrinsic $f_{max} = 200$ GHz and extrinsic $f_{max} = 106$ GHz	[33]
	DNA biosensor	CVD	Liquid gate and PDMS well to isolate source/drain electrodes	Detection of full hybridization of the complementary strand down to 15 aM	[34]
Back gated	Study of velocity saturation: design and performance	Pulsed CVD	Use the h-BN as a gate oxide. Dual-gate device	$\frac{f_{max}}{f_T} > 5$	[35]
	Achieve high f_{max}	CVD	Buried gates to reduce gate resistance	Intrinsic $f_T = 35$ GHz and $f_{max} = 50$ GHz	[36]
	Achieve high f_{max}	CVD	T-gate structure to reduce the gate resistance	Extrinsic $f_T = 11.4$ GHz and $f_{max} = 15$ GHz	[37]
	Improvement of the process-induced mobility degradation of graphene	CVD	Development of buried gates	$I_{on}/I_{off} = 5.31$ Maximum $g_m = 6.85\ \mu S\ \mu m^{-1}$ Intrinsic $f_T = 2$ GHz and $f_{max} = 13$ GHz	[38]
	High-sensitivity label-free DNA biosensor	CVD	Electrolysis bubbling method for graphene transfer	The detection limit depends on the length of the DNA	[39]
	Graphene FET biosensor for the label-free sensing of exosome	CVD	Back gate contact made with silver paint	Exosome detection of at least 0.1 $\mu g\ ml^{-1}$	[40]
Top/back gated	GFET	Mechanical exfoliation	Gate oxide (Al_2O_3) deposited by ALD	Preservation of graphene mobility after gate dielectric deposition ($8000\ cm^2\ V^{-1}\ s^{-1}$)	[41]
	Frequency doubler	Mechanical exfoliation	Yttrium oxide as gate dielectric	Able to work with 200 kHz input frequencies	[42]
	RF applications	Mechanical exfoliation	h-BN used as top and back gate dielectric	Current density of $1.2\ A\ mm^{-1}$ Extrinsic $f_T = 33$ GHz	[43]

Source: Adapted from Jmai et al. [26].

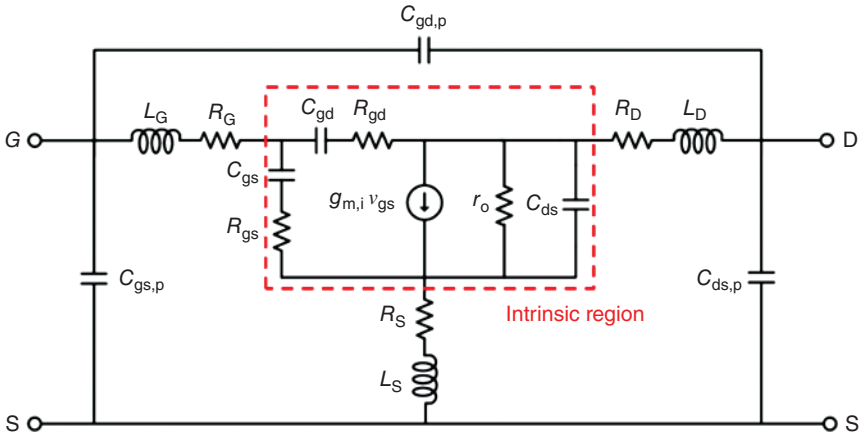

Figure 1.8 Small-signal equivalent circuit model of FETs.

Bearing this in mind, many papers try to achieve the closest and most reliable GFET model possible. Like all transistors, GFETs can be modeled using the small-signal model, shown in Figure 1.8, and that is what is done in [45]. This is an empirical model and is composed of a current source, I_{ds}, an output resistance, r_o, gate resistance and inductance, R_g and L_g, drain resistance and inductance, R_d and L_g, source resistance and inductance, R_s and L_s, drain to source capacitance, C_{ds}, gate to drain capacitance and resistance, C_{gd} and R_{gd}, and gate to source capacitance and resistance, C_{gs} and R_{gs}. The resistances and inductances associated with the terminals alone raise from their geometrical design. The capacitances and resistances between the GFET terminals appear due to the devices' small size and must be considered for the high-frequency domain. It is well known that the transconductance, g_m, is the slope of I_{ds} against V_{gs} $\left(g_m = \frac{dI_{ds}}{dV_{gs}} \right)$. Therefore, most of the time I_{ds} appears as the product of g_m and V_{gs}. Because this is an empirical model all parameters can be extracted from the measurement of the S parameters and DC analysis. The DC analysis consists in measuring I_{ds} while changing V_{gs}. This allows for a draft of the DC characteristic of the GFET and obtaining the corresponding g_m. The other parameters can be obtained from the Y parameters (standard conversion from the S parameters) using the following expressions:

$$D = 1 + w^2 C_{gd}^2 R_{gd}^2 \tag{1.5}$$

$$C_{gd} = -\frac{\mathrm{Im}\left(Y_{12}\right)}{w} \cdot \left[1 + \left(\frac{\mathrm{Re}\left(Y_{12}\right)}{\mathrm{Im}\left(Y_{12}\right)} \right)^2 \right] \tag{1.6}$$

$$R_{gd} = \frac{\mathrm{Re}\left(Y_{12}\right)}{\mathrm{Im}\left(Y_{12}\right)} \cdot \frac{1}{wC_{gd}} \tag{1.7}$$

$$R_{gs} = \frac{\mathrm{Re}\left(Y_{11}\right) - \dfrac{w^2 C_{gd}^2 R_{gd}}{D}}{\mathrm{Im}\left(Y_{11}\right) - \dfrac{wC_{gd}}{D}} \cdot \frac{1}{wC_{gd}} \tag{1.8}$$

$$C_{ds} = \frac{\mathrm{Im}\left(Y_{22}\right)}{w} - \frac{C_{gd}}{D} \tag{1.9}$$

$$C_{gs} = \frac{1}{w} \cdot \left[\mathrm{Re}\left(Y_{11}\right) - \frac{w^2 C_{gd}^2 R_{gd}}{D} \right] \cdot \left[\frac{\mathrm{Im}\left(Y_{11}\right) - \dfrac{wC_{gd}}{D}}{\mathrm{Re}\left(Y_{11}\right) - \dfrac{w^2 C_{gd}^2 R_{gd}}{D}} + \frac{\mathrm{Re}\left(Y_{11}\right) - \dfrac{w^2 C_{gd}^2 R_{gd}}{D}}{\mathrm{Im}\left(Y_{11}\right) - \dfrac{wC_{gd}}{D}} \right] \tag{1.10}$$

In this chapter, the authors use a fixed g_m to simulate the S parameters, and because of that the generalization of this model becomes difficult since operating the GFET at the Dirac point is especially important to some applications, like the ring oscillator, and close to this point g_m changes a lot.

In [46], the authors take a different approach. Instead of relying only on measured data, they try to predict the transistor behavior using analytical expressions as well as some tabulated values of the materials' properties. With their work, the authors were able to implement a compact equivalent circuit that evaluates the value of I_{ds} in the three working regions and verified the model against experimental DC data. The major difference between both models here presented, is that one relies on measured data to analyze RF performance, and the other using only theoretical data to predict the DC behavior of the transistor.

Reported in the literature are several models that try to predict the behavior of the GFET, and by taking different approaches, they can predict its behavior in a closed operation zone. To replace silicon, the GFET model needs to be standardized in all operation zones, allowing researchers and chip manufacturers to design and predict the device performance accurately.

The FOMs of GFETs are the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}). The f_T is defined as the frequency at which the magnitude of the small-signal current gain is unitary ($h_{21} = 0$ dB). This FOM is usually extracted from the h_{21} parameter, which is obtained by the measurement and conversion of the S parameters of the device, using the following expression:

$$h_{21} = \frac{-2S_{21}}{\left(1 - S_{11}\right)\left(1 + S_{22}\right) + S_{12}S_{21}} \tag{1.11}$$

Also, to predict the cut-off frequency, it is generally used the following expression:

$$f_T = \frac{g_m}{2\pi\left[\left(C_{gs} + C_{gd}\right)\left(1 + \left(R_d + R_s\right)g_{ds}\right) + C_{gd}g_m\left(R_d + R_s\right) + C_{pg}\right]} \tag{1.12}$$

$$k = \frac{1 + \left|S_{11}S_{22} - S_{12}S_{21}\right|^2 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2}{2\left|S_{12}\right|\left|S_{21}\right|} \equiv \text{Stability Factor} \tag{1.13}$$

The f_{max} is described as the frequency when the maximum available power gain (MAG/MSG) becomes unitary (MAG/MSG = 0 dB). This gain is not directly calculated, it must satisfy some conditions. By using the S parameters, the first thing to evaluate is the stability factor for all frequencies using the following expression:

$$U = \frac{\left|\frac{S_{12}}{S_{12}} - 1\right|^2}{2k\left|\frac{S_{21}}{S_{12}}\right| - 2\,\mathrm{Re}\left(\frac{S_{21}}{S12}\right)} \equiv \mathrm{Mason's\,Gain} \tag{1.14}$$

Afterward, comes the evaluation of all k's. If all k's are less than one ($k<1$ for all frequencies), the MAG/MSG corresponds to the Mason's Gain, and it can be calculated using the following expression:

If all k's are not less than one, for each frequency must be evaluated if k is less or greater than one. If k is less than one ($k<1$), the MAG/MSG corresponds to the maximum stable gain, and can be calculated using the following expression:

$$\mathrm{MSG} = \frac{\left|S_{21}\right|}{\left|S_{12}\right|} \equiv \mathrm{Maximum\ Stable\ Gain} \tag{1.15}$$

If k is greater than one ($k>1$), the MAG/MSG corresponds to the maximum available gain, and can be calculated using the following expression:

$$\mathrm{MAG} = \mathrm{MSG}\left(k - \sqrt{k^2 - 1}\right) \equiv \mathrm{Maximum\ Available\ Gain} \tag{1.16}$$

Finally, the MAG/MSG can be converted to dB by the evaluation of 10 times the logarithmic of each value of MAG/MSG (MAG/MSG (dB) = $10\log_{10}$(MAG/MSG)).

Like for f_T, there is a general expression used to try to predict f_{max}, and it is the following:

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}\left(R_g + R_s\right) + 2\pi f_T R_g C_{gd}}} \tag{1.17}$$

1.5 2D Material Diodes

A diode is an electronic component that allows current to flow in one direction while it blocks transport in the reverse direction, thus rectifying the electric signal. The most common type of semiconductor diode is a p–n junction. The p–n junction induces an electric field in a space-charge carrier with a depleted volume, which enables current rectification. There are homo- and heterojunctions, depending on whether both sides of the junction are made of the same or different materials. 2D materials junctions can be made 2D or 1D. Certain authors add a gate to the junction diode, to tune the chemical potential on one or both sides of the junction, thus improving the device performance.

1.5.1 Most Common Topologies

P–n junctions based on 2D materials can be made of only one material (*2D homostructures*), two different materials (*2D heterostructures*), or different dimensions materials (*mixed dimensional*) [47]. 2D homostructures can be obtained using different methods, shown in Figure 1.9, which are as follows:

- *Thickness based*: p and n regions are formed by regions with different thicknesses.
- *Electrostatically doped*: p and n regions are obtained using local gates.
- *Chemical doping*: p and n regions obtained by the surface adsorption of molecules, nanoparticles, or quantum dots.
- *Elemental doping*: two flakes with different doping are stacked.

2D heterostructures can be:

- *Vertical*: stacking two different 2D materials on top of each other.
- *Lateral*: combining two different 2D materials on the same plane.

Mixed dimensional can be:

- *2D–0D and 2D–1D*: 2D–0D and 2D–1D material junctions.
- *2D and 3D*: stacking of 2D and 3D material on top of each other.

A thickness-based diode using MoS_2 is reported in [48], with a rectification ratio of $\approx 10^3$ and a small ideality factor (a value that compares the diode with the ideal diode) of 1.95. Besides the good electronic properties, it also has good photoresponsivity of $10\,A\,W^{-1}$ and high photosensitivity of 10^5.

In [49], it is reported that two different mixed dimension-based diodes are similar to metal-insulator-metal (MIM) diodes, but one of the metals is replaced by graphene, creating a metal-insulator-graphene interface (MIG), as shown in Figure 1.10. The difference between both approaches is the type of interface between graphene and the insulator, being a 2D or 1D interface, shown in Figure 1.11. From the 2D to 1D interface, the capacitance and series resistance decrease, allowing to fully exploit the high mobility of graphene, which increases the device cut-off frequency (predicted to be up to 2.4 THz) and current density (from 7.5 [50] to $7.5 \times 10^6\,A\,cm^{-2}$ [51]).

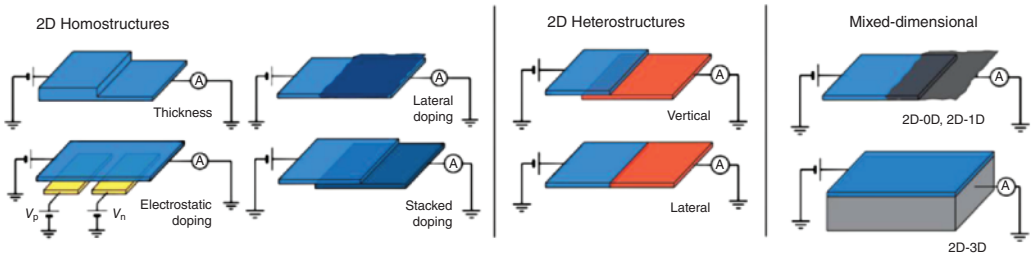

Figure 1.9 Schematic of different p–n junctions. Source: Adapted from [42].

Figure 1.10 Schematic of the 2D (left) and 1D (right) MIG diodes. Source: Wang et al. [49]/ John Wiley & Sons.

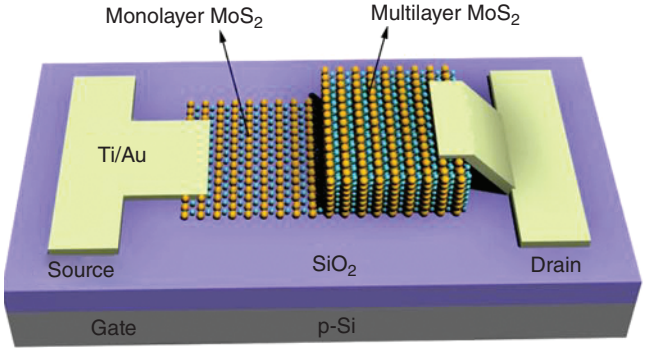

Figure 1.11 Schematic of the thickness-based diode. Source: Sun et al. [48]/Springer Nature/CC BY 4.0.

1.5.2 Modeling of 2D Materials-Based Diodes

The modeling of 2D material diodes has not been well explored, so modeling such devices relies on parameter extraction. In [52], it is described as a small signal equivalent, Figure 1.12, that is composed of a linear capacitance, C_1, and nonlinear bias-dependent capacitance, C_2, two leakages variable resistances, R_1 and R_2, and the

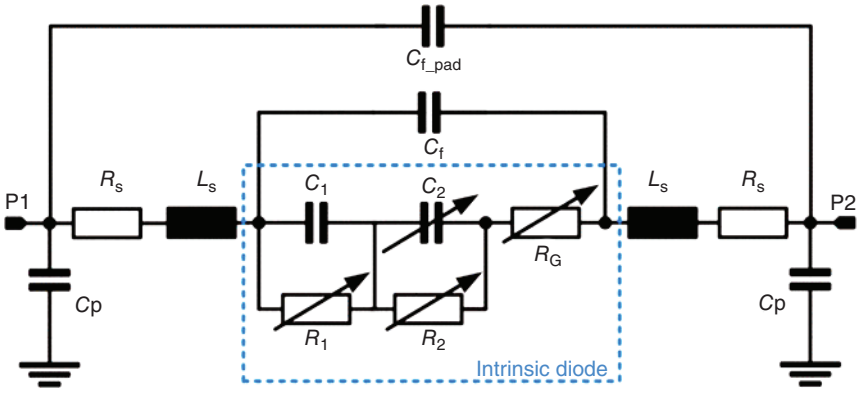

Figure 1.12 Small-signal equivalent circuit model of diodes.

graphene sheet resistance, R_G. In addition to the intrinsic region, the model also includes extrinsic parasitics.

1.6 Graphene Devices

Due to the high conductivity of graphene, GFETS can have large values of f_T and f_{max}. Therefore, GFETs are becoming the focus of much research for RF devices like frequency multipliers, mixers, and oscillators.

1.6.1 Graphene Frequency Multipliers

Due to the V-shaped transfer curve of GFETs, it is possible to obtain a frequency doubler when operating at the Dirac point. In simple terms, if a signal with DC bias equal to the Dirac point of the transistor is applied to the gate, V_{gs}, the output current I_{ds} has double the frequency.

In [42], a top/back-gated against back-gated frequency doubler is studied, showing a significant improvement in the operating frequency from 10 to 200 kHz when the top gate is added to the back-gated device. For the top/back-gated device, the output power is concentrated at 400 kHz with a relative power of 75% Another frequency doubler on a flexible substrate is reported [53], which achieved a spectral purity higher than 97% and a high conversion gain of −13 dB.

A W-shaped transfer curve is obtained when two GFETs with different Dirac points are combined in series. When operating at different points of the W-shape it is possible to obtain a frequency tripler or quadrupler. A frequency tripler is reported in [54] with spectral purity higher than 70% at an output frequency of 600 Hz.

A different approach is implemented in [55, 56], where the W-shaped transfer curve is achieved with a single GFET by biasing the back and top gates of top/back-gated transistors. In [55], a frequency tripler is studied, and a device with spectral purity higher than 90% was achieved at an output frequency of 3 kHz. In [56], a frequency quadrupler with spectral purity of 50% at 800 kHz was reported.

1.6.2 Graphene Mixers

It is reported in [57] that it is possible to implement an RF mixer with operating frequencies up to 10 GHz while having a high conversion loss of 30 dB at 1 GHz using a single GFET. Another graphene RF mixer is studied in [58], where frequencies up to 10 GHz and excellent thermal stability were achieved, with its peak performance around 4.5 GHz and a conversion loss of 27 dB. In [59], the authors study the effects of reducing channel length on the graphene mixer. With this study, the authors concluded that the conversion loss increases by reducing the channel length while the IIP3 increases.

1.6.3 Graphene Oscillators

1.6.3.1 Ring Oscillators

Another implementation of graphene transistors is reported in [60]. In this chapter, the authors propose the implementation of GFETs as a ring oscillator. A ring oscillator is a circuit built of an odd number of cascaded logic inverters in a loop. This loop induces instability and therefore induces oscillations at high frequencies. Each inverter must be identical, and over-unity voltage gain $\left(A = \frac{g_m}{g_{ds}} > 1 \right)$ is required. The FOM used for this kind of device is the maximum oscillation frequency, f_O, since it is smaller than f_T. Although the positive voltage of the drain induces a shift on the Dirac point [61], the complementary GFETs of the inverters were obtained by using a back gate voltage to ensure a proper shift of the Dirac point. In this study, the authors made three types of devices: large ($L = 3$ μm and $W = 20$ μm), medium ($L = 2$ μm and $W = 10$ μm), and small ($L = 1$ μm and $W = 10$ μm), obtaining 284 MHz $< f_O <$ 350 MHz, 504 MHz $< f_O <$ 750 MHz, and 1 GHz $< f_O <$ 1.28 GHz for each device, respectively.

A similar ring oscillator is presented in [62], in which the authors also studied the effects of changing the transistors' channel size, access length, and source and drain contact thickness. The best device achieved a $f_O = 4.3$ GHz.

1.6.3.2 LC Tank Oscillators

Although full graphene-based LC tank oscillators have not been accomplished yet, the implementation of graphene inductors, capacitors, and transistors alone to study their performance in LC tank oscillators has been reported.

The capacitor developed in [25] was implemented in an LC tank by adding a 2 mH inductor in series, achieving a tunable resonant tank from 1.45 to 1.73 MHz and a Q-factor ranging from 65 to 25.

In [63], the performance of a graphene LC tank used in an oscillator was assessed through simulation. This simulation relied on graphene capacitor and inductor values found in the literature, and an oscillation frequency of 1.5 GHz was achieved with a phase noise of $-134\,\text{dB}\,\text{Hz}^{-1}$.

1.7 Conclusion

From the gathered information in this writing, it is possible to conclude that the research on 2D materials has a long way to go. Although graphene is the most researched 2D material and shows excellent electronic properties to outperform silicon devices in certain applications, state-of-the-art in devices' fabrication and modeling predictions have yet to be well established. Moreover, the devices' performance reported in the literature shows excellent potential to improve or substitute RF circuit designs, but more research on this matter needs to be conducted to assess the true potential of such devices.

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