1 Introduction

1.1. Motivation

Recently, a variety of commercial and defense applications that demand for sub-Terahertz and mm-wave integrated circuits have emerged [1]. The frequency range between 100 GHz and 1 THz offers large bandwidth for high-speed communications as well as improved performance of sensors and imaging systems due to short wavelengths. All these systems require signal sources for local oscillators or signal generation. The sources are key building blocks for such applications. Performance targets include particularly a combination of high output power, low phase noise and high DC-to-RF efficiency. In the past years, significant progress has been made in sources for the mm-wave and sub-terahertz frequency range, using various semiconductor technologies. Mostly, these sources have been realized in push-push configuration [2], [3]. Few of them are fundamental frequency sources [4], [5] but they are relatively power-hungry and deliver less output power. Hence, developing efficient fundamental frequency sources at sub-THz and mm-wave frequencies is still the subject of intensive research.

Integrated sources based on frequency multiplication offer many advantages for mm-wave and THz frequencies applications. At present, in the microwave frequency bands fundamental sources are commercially available and mature enough offering high output power and efficiency, low noise, electronic tuning and compact design [6], [7]. Usually, millimeter-wave and terahertz frequency multipliers exhibit broadband, high power handling capabilities and high efficiency. Therefore, a microwave source combined with a millimeter-wave or terahertz frequency multiplier provides a compact broadband tunable source at frequencies from 30 GHz to well above 1 THz [8], [9].

The major challenge in signal generation at such frequencies is that the active devices have to be operated close to, or even above their transit frequencies and close to breakdown voltage as well. Additionally, the quality factor of the passive components degrades compared with lower frequencies. Recently, SiGe and CMOS circuits have been demonstrated operating at frequencies beyond 250 GHz [10], [11]. Nevertheless, due to their more relaxed geometrical dimensions, compound semiconductors such as InP offer better power capabilities. This is why InP is used in the research work presented here.

But it is not sufficient to have individual circuits with decent performance. Integrated components and modules with increased functionality are crucial for successful implementation of system on-chip solutions. At millimeter-wave and THz frequencies system-on chip solutions further improve performance because the number of interconnects is reduced. Nowadays, system-on chip solutions based on CMOS and BiCMOS technologies cover both analog and digital circuits and reach operating frequencies beyond 250 GHz [12], [13]. However, this is achieved at the cost of lower breakdown voltage and thus reduced output power. On the other hand, compound semiconductors such as InP exhibit operating frequencies approaching 1 THz with high power capabilities [14]. Therefore, wafer-level hetero-integration of InP circuits with BiCMOS promises great potential. This is a main motivation behind the research work presented here. Recently, research on InP-on-BiCMOS device level integration has been reported by the DARPA funded consortium [15], [16] and there are ongoing activities to combine GaN-on-Si CMOS [17].

1.2. Research Objectives

This thesis investigates realization of signal sources for the frequency range beyond W band in InP TS-DHBT and InP-on-BiCMOS technologies. Since the transferred-substrate process has been made available only recently, emphasis of the work is on exploring capabilities in terms of performance and demonstrating the potential of the hetero-integration technology. The specific research objectives include:

- Design and characterize fundamental and harmonic fixed-frequency oscillators up to 300 GHz using the InP TS process.

- Design and characterize signal sources based on multipliers for frequencies beyond 200 GHz using the InP TS process as well as the InP-on- BiCMOS versions.

1.3. Thesis Organization

The dissertation is organized as follows: Chapter 2 discusses the InP TS process and the hetero-integrated InP-on-BiCMOS process technology. Chapter 3 describes the active and passive modelling as well as measurement methodology. Chapter 4 presents the general theory of oscillators as well as the design and measurement results of the oscillators in InP TS and InP-on-BiCMOS process technology.

Chapter 5 then is devoted to the circuit topologies and the measured results of the various frequency multipliers developed. Chapter 6 deals with the details of the design procedure and the results of the hetero-integrated signal sources. At the end, Chapter 7 summarizes the contributions of the research work presented in this dissertation and gives an outlook for future designs at mm-wave and THz frequencies.

2 Technology

Still growing needs for faster data communication rates and to fill up new application areas up to Terahertz (THz) frequencies raise the question how far traditional semiconductor technologies can satisfy these markets. To address this challenge, advanced semiconductor devices with maximum oscillation frequencies (f_{MAX}) of 1 Terahertz or beyond have been developed [18]. Device scaling plays the most important role in this journey. Si technologies based on Si CMOS or SiGe BiCMOS HBTs are preferred for various applications owing to the high integration level, mature design environment, low power and low cost (for high volume). However, its device operation speed is limited by the intrinsic material properties of Si. In contrast, high speed III-V technologies based on GaAs or InP benefit from excellent electron transport characteristics such as high mobility and speed. This is clearly shown in Fig. 1, which compares recently reported unity current gain, f_t and unity power gain, f_{MAX}; values of various III-V and Si-based devices. It is obvious from the plot that the speed of III-V devices, both HBTs and HEMTs, dominate over that of Si devices, exhibiting best f_{MAX} exceeding 1.2 THz. It is also true that the operation speed of Si-based devices has been significantly improved over the past years, now reaching up to 500 GHz (see Fig. 2.1) in terms of f_{MAX}, which is sufficient for circuits operating well beyond 100 GHz. This is achieved with aggressive device scaling, which increases mask and processing cost. This aggressive device scaling significantly reduces the breakdown voltage and hence the available RF output power. On the other hand, compound semiconductors such as InP exhibit high power capabilities at operating frequencies beyond 200 GHz. This is also clearly visible in Fig. 2.2, which shows recent power trends realized in various circuits on different technologies.

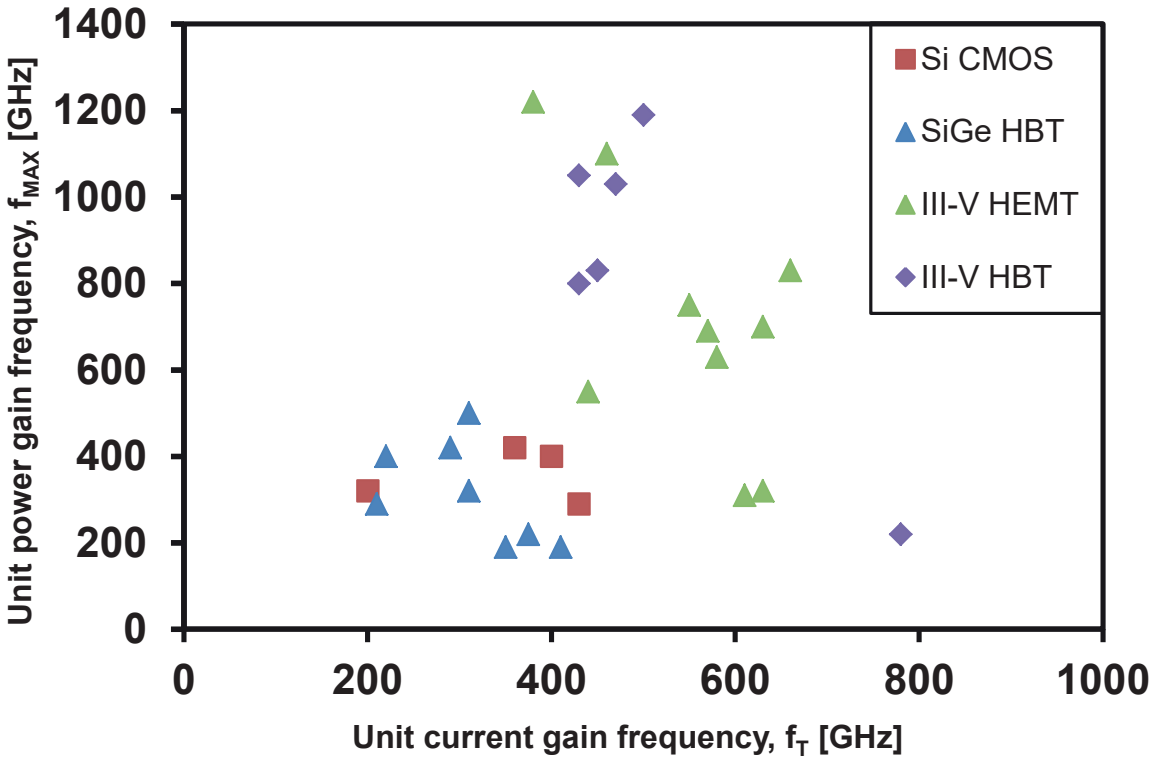

Fig. 2.1. f_T and f_{MAX} of recently reported devices achieved on different technologies [19].

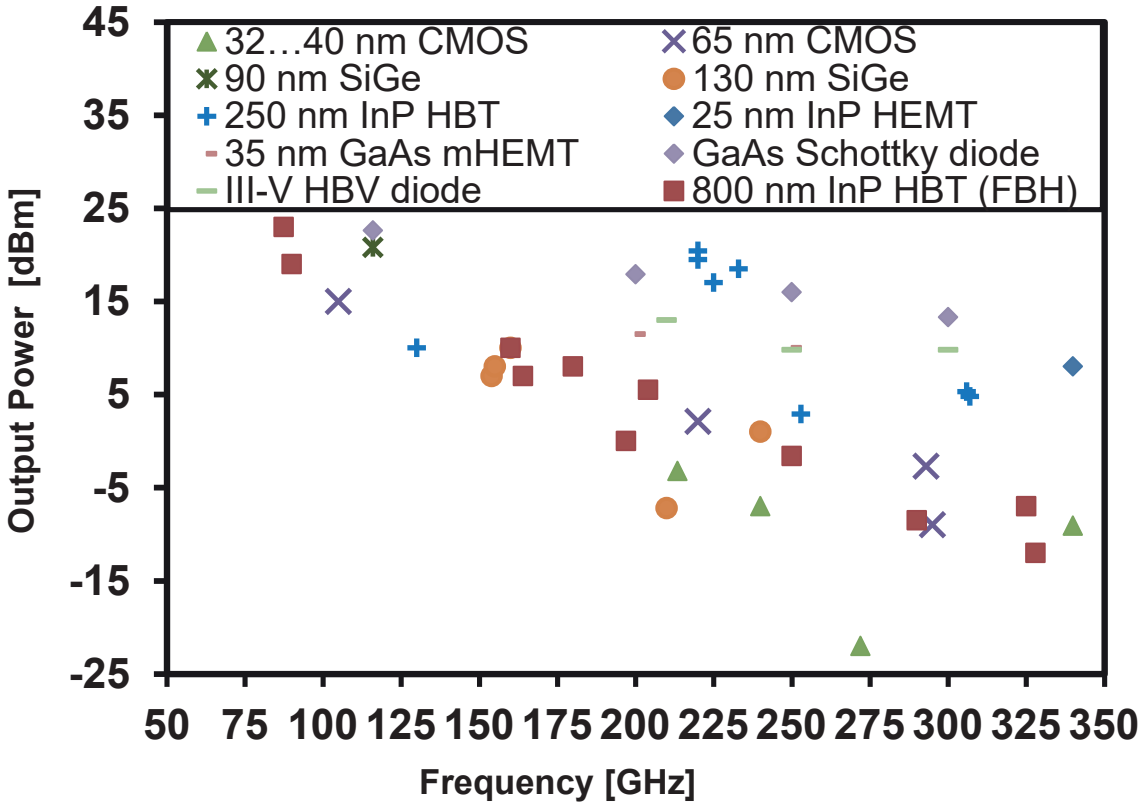

Fig. 2.2. Performance of recently reported circuits operating near or beyond 100 GHz on different technologies.

The III-V based devices achieve higher f_T and f_{MAX} values and they deliver higher output power compared to the Si-based technologies. But, their capability in terms of circuit complexity and functionality is lower than for the Si technologies, i.e., CMOS or SiGe BiCMOS. Therefore, combining Si based technologies with a III-V compound semiconductor such as InP offers the possibility to realize compact circuits with benefits from both technologies. This solution combines the high-integration capabilities of the silicon process and the high-frequency high-power potential of compound semiconductor (see Fig. 2.3). Such integrated components and modules with increased functionality are crucial for successful implementation of system-on-chip solutions. At millimeter-wave frequencies and beyond system-on-chip solutions show superior performance compared to other approaches, due to the reduced number of chip-to-chip interconnects in the systems, which become increasingly lossy at high frequencies.

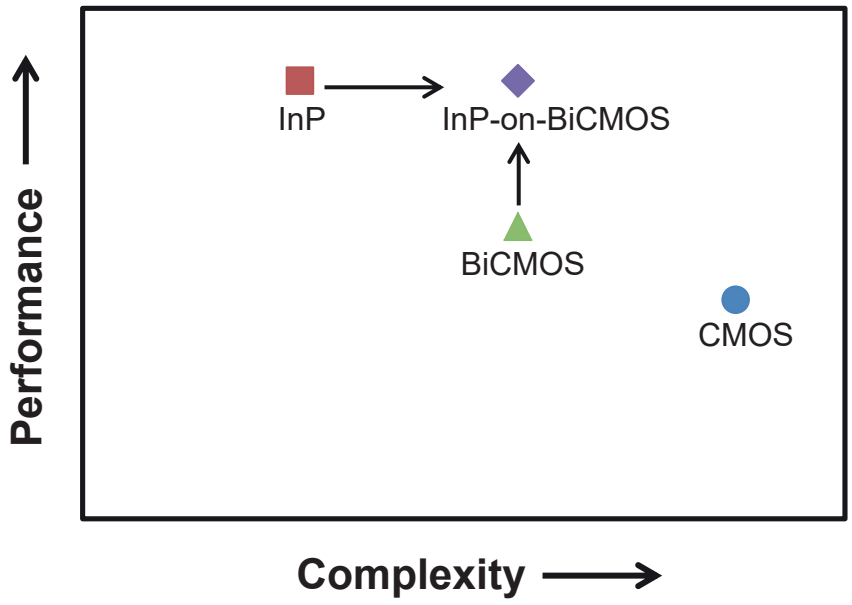

Fig. 2.3. Performance vs complexity in different technologies.

In this work, the main focus is on circuit designs for the FBH 0.8 µm transferred-substrate (TS) InP-DHBT process. The transfer of the substrate, i.e. removing the InP, embedding the HBT in BCB and using AIN as a host substrate, offers several advantages: less extrinsic capacitance, relaxed geometry and better heat conduction by means of replacing InP substrate by AIN substrate. The TS InP-DHBT process flow is briefly discussed in Section 2.2 while Section 2.3 describes the heterogeneous (InP-on-BiCMOS) process.

2.1 Transferred Substrate (TS) Process Flow

The TS InP DHBT epitaxial layer composition is similar to conventional DHBTs, but with reduced sub-collector thickness and additional etch stop layers at the bottom for substrate removal. The first step, the front-side process, is the same as for conventional InP-DHBTs. In this step, base and emitter metal is introduced, then emitter mesa is etched and at the end the base metal is deposited. After that, planarization of the device is done by benzocyclobutene (BCB) and then the ground metallization is formed. This completes the front-side process (see Fig. 2.4. a). In the next step the complete structure is bonded upside down onto an AlN wafer with a 2-µm layer of benzocyclobutene (BCB) (see Fig. 2.4. b). After curing the BCB the two wafers form a firm compound. Then the whole structure is flipped as shown in Fig. 2.4. c and the InP substrate including all unnecessary semiconductor material (e.g., the extrinsic collector under the base contacts and base pad) are removed by etching back-to-front, until only the epitaxial layers of the active circuit elements remain. This approach substantially reduces device parasitics, since the transistor is embedded in BCB (ε_r=2.65) instead of InP (ε_r=11). Thus, operating frequency is increased without transistor downscaling. These features of the transferred-substrate technology make it ideally suited for high-frequency power applications. After removing the InP substrate, collector mesa is etched. At this step, the collector metal is open to access, which can be independently scaled according to the electrical and thermal requirements (see Fig. 2.4. d). In a final step, necessary vertical interconnects are formed and base metal resistor, MIM capacitors (dielectric material: SiNx) and thin-film microstrip transmission lines complete the TS MMIC process. Fig. 2.5 shows the schematic cross-section of the final InP TS DHBT process structure. The TS version used in this work is based on a 0.8 µm InP-DHBT technology, which offers f_T/f_{MAX} values above 320 GHz with BVCEO = 4V [20]. The process has three Au metal layers with 1µm, 1.5µm and 4.5 µm thickness, respectively, with a dielectric constant of 2.65. For more details of the TS process flow see [20].