Introduction of Fraunhofer IZM's and TU Microperipheric's Activities

Location in Berlin-Wedding

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Forschungsschwerpunkt
Technologien der Mikroperipherik

Fraunhofer IZM

Fraunhofer IZM – Facts

Figures 2014

- appr. 30 Mio. € turnover
- appr. 80 % contract research
- 389 employees
  (230 full time, 159 PhD, trainee)

Locations

- Berlin
- Oberpfaffenhofen
- Dresden-Moritzburg

Director

Prof. K.-D. Lang

University Cooperation

- Long term contract with Technical University of Berlin
- Research Center Microperipheric Technologies
- Approx. 100 additional staff
- Joint use of equipment, facilities and infrastructure
- Additional cooperation with Technical University Dresden (assistant professor)

- Material characterization
- Process evaluation
- Reliability testing
- Failure analysis
- Sample production
- Training courses

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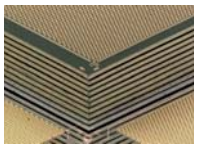
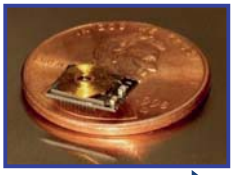
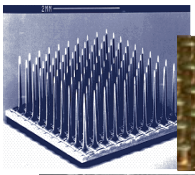
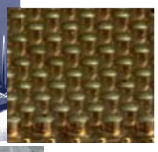
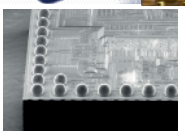
Mission: From Microelectronics and Microsystems towards Smart Systems

System Integration Technologies

Multifunctionality
System Reliability
Adapted Formfactor
Low Cost


[nm], [µm] — Nanodimensions — to — [m] — Final Product Size

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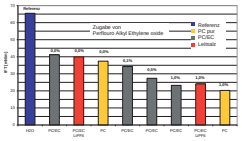
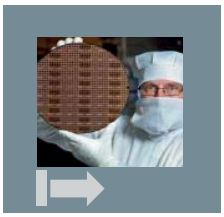
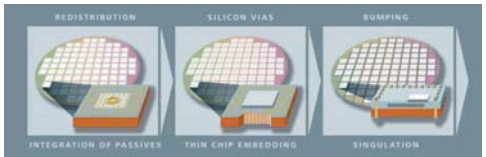
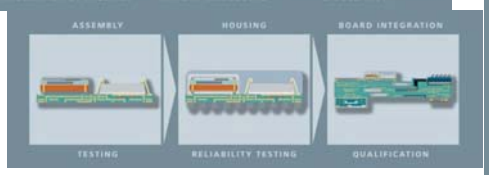
Main Competencies



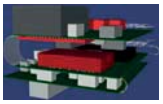
Environment oriented
Material/Energy/
Lifetime Assessment

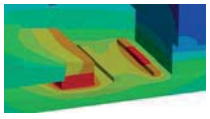


2D/3D Waferlevel Technology
Thin Film (Metal, Polymer)
MEMS Structures

2D/3D Panellevel Technology
Micro-Interconnects
Assembly and Packaging



2D/3D Technology Design
Sensor Nodes, Power and
System Design



Mechanical and thermal Reliability
Molecular Modeling
Micro Nano Analysis
Simulation

Micromechatronics
Mechanical Interconnects
Process Simulation
Harsh Environment Analytics

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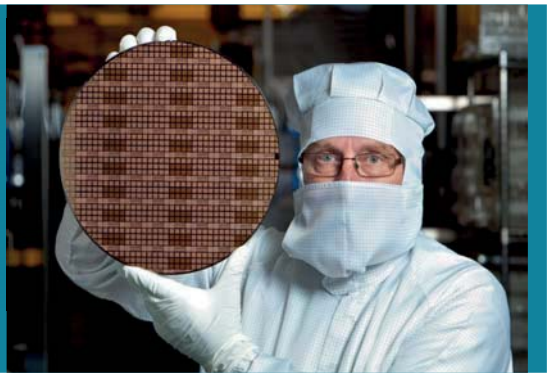
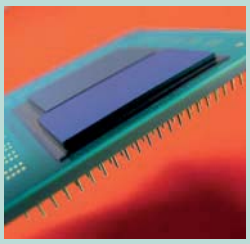
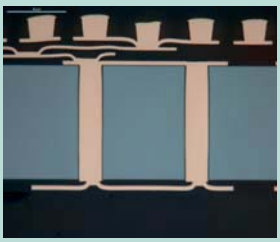
Solutions with Wafer Level Packaging

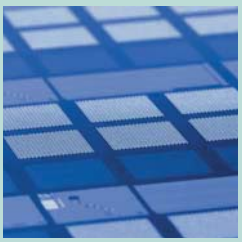
3D Wafer Level Systemintegration

- Through Silicon Via (TSV) Formation
- Wafer thinning, Thin Wafer Handling
- TSV Interposer with high-density metallization
- Assembly and interconnection technologies









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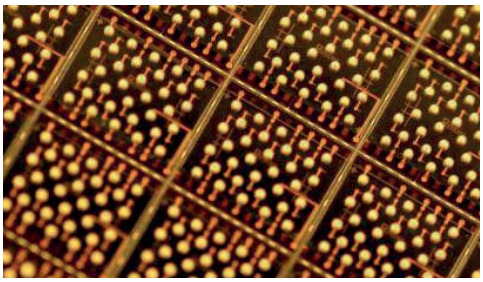
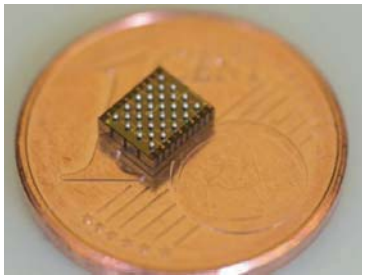
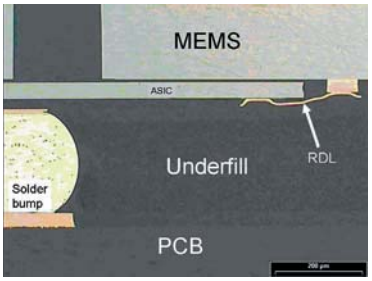
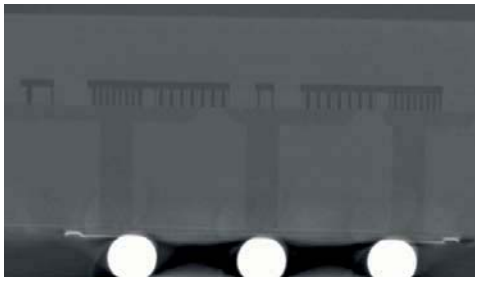
Example: MEMS Sensor Integration

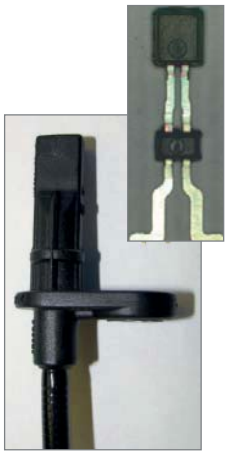
Thin Chip Integration on Gyro (Capping Wafer with TSV)











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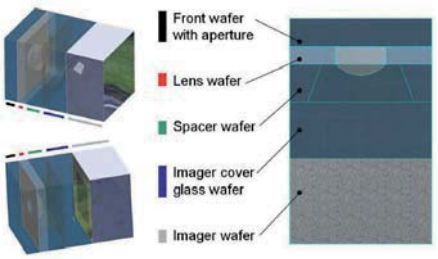
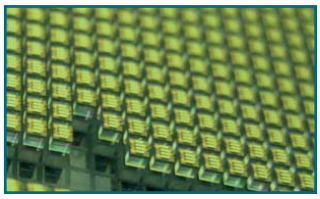
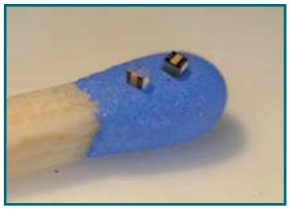
Example: Wafer Level Integration for a Microcamera

- Wafer level integration of optics and camera electronics
- Size: 1,0 x 1,0 x 1,0 mm³
- Application e.g. for low-cost endoscopy







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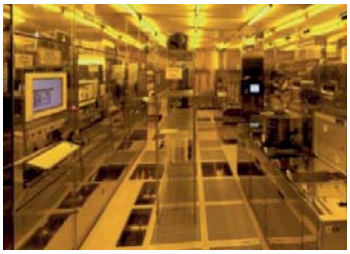
3D Waferlevel Infrastructure

Cleanroom Conditions like Semiconductor Production



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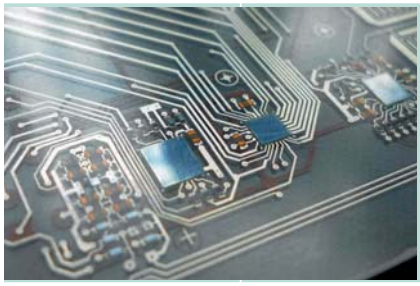
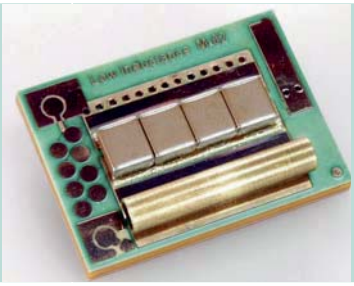
Tagungswebsite:
https://photonik.hs-harz.de/groups/xiiitgworkshopoptischekomponentenfurclouddatacenterimfraunhoferizmberlin/

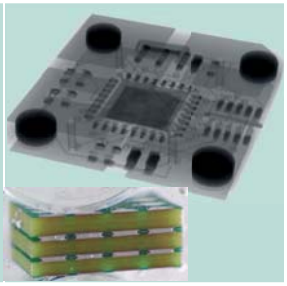
Solutions with Panel Level Packaging

Panel Level Systemintegration

- High density wiring
- High K and low K **dielectrics**
- Thin chip handling and assembly
- Ultra thin interconnects
- Embedded actives and passives
- Functional layer integration







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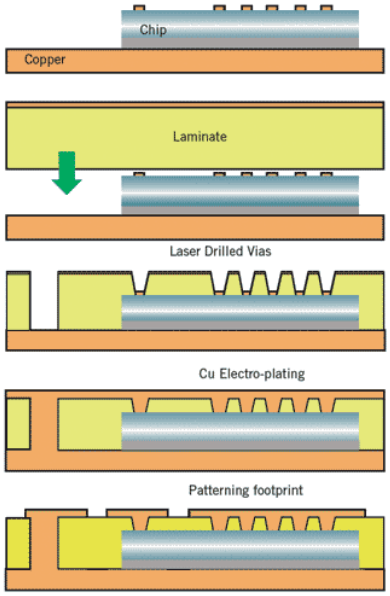
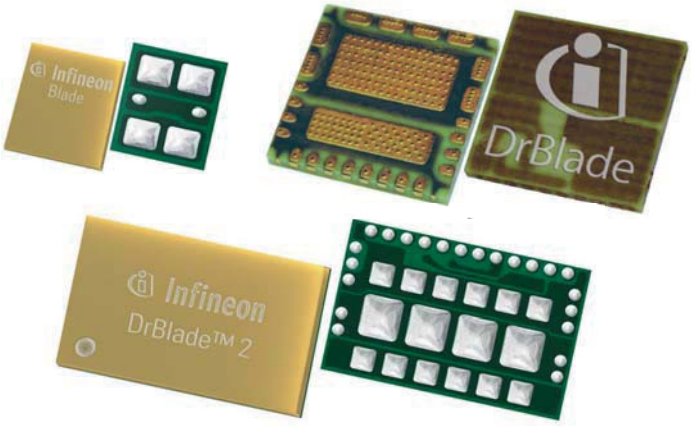
Chip Embedding Technologies

Process Flow



Example: Blade (INFINEON)

- embedded MOSFET / Driver
- manufacturing on PCB format



Licensing and process transfer
from Fraunhofer IZM

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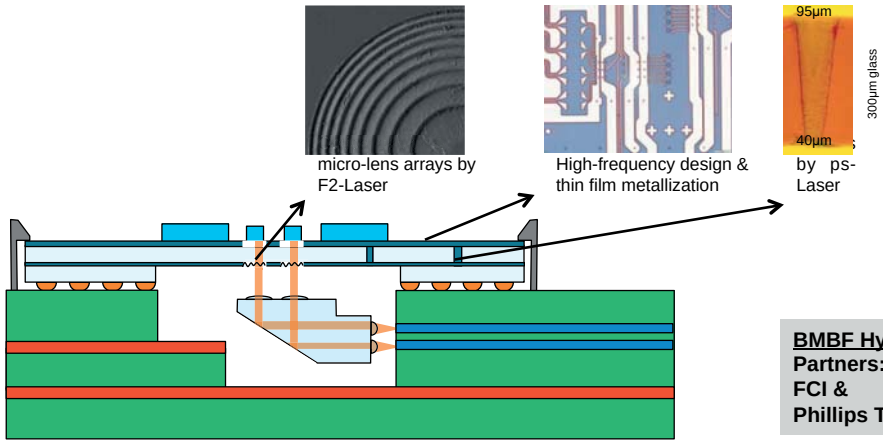
Optical interconnects moving closer to CPU and memory

- Replacing electrical high-speed data interconnects by optical interconnects on board-level
- Development of mid-board electro-optical transceivers
- Glass interposer with through glass vias (TGVs), electrical HF design and thin film metalization and fresnel micro-lens arrays



BMBF HyPOT Project
Partners:
FCI &
Phillips Technologie

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Panel Level Systemintegration - Infrastructure






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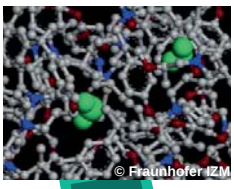
System Design and Reliability

Interdisciplinary Technology Levels that have to be Considered

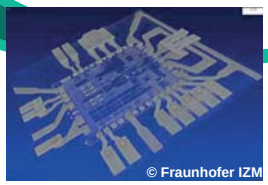
Material Level for Physical Characteristics



Product as Superordinate System

Interconnect Level for Technological Characteristics

Chip Level for Design Characteristics



Board Level for Interdependency

Module Level for Environmental Interaction

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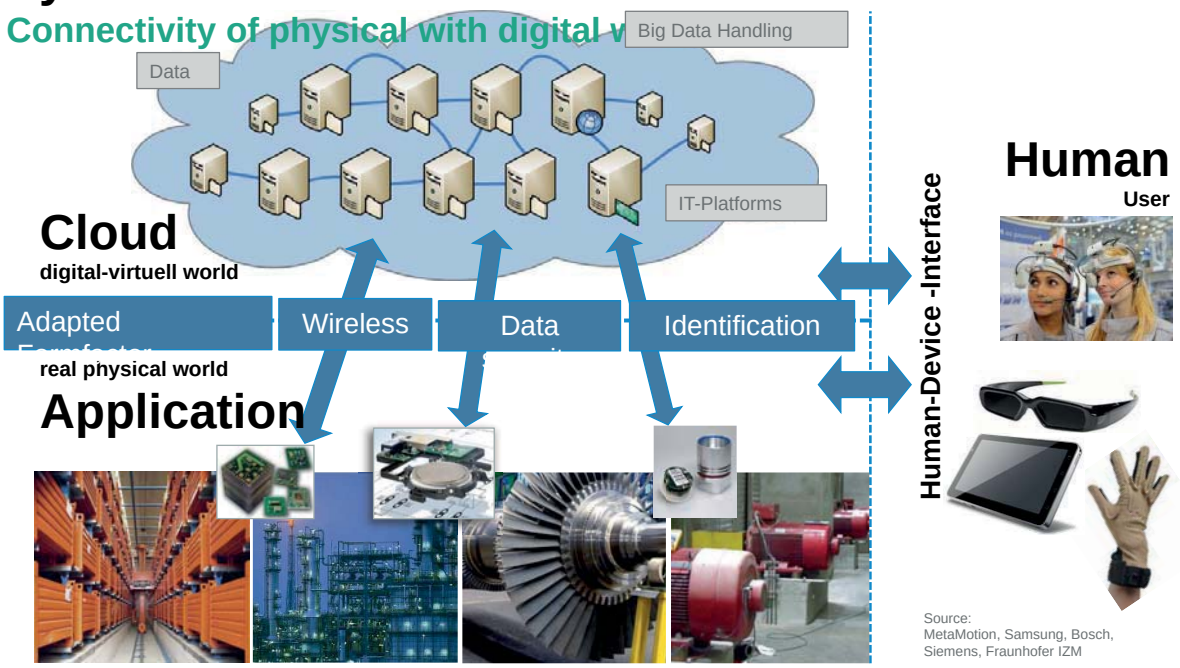
Future Systemintegration - Cyber-Physical Systems

Connectivity of physical with digital v



Source:
MetaMotion, Samsung, Bosch, Siemens, Fraunhofer IZM

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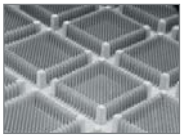
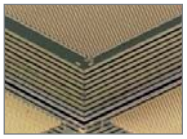
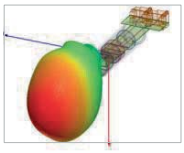
THANK YOU FOR YOUR ATTENTION

Contact:
Prof. Dr.-Ing. Dr. sc. techn. Klaus-Dieter Lang
kdlang@izm.fraunhofer.de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Migration of Optical Interconnect into Sub-TOR Data Centre Subsystems
Richard Pitwon, Seagate GB

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