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Vapor Phase Growth of Metal-Oxide Thin Films and Nanostructures

Lynette Keeney and Ian M. Povey

University College Cork, Tyndall National Institute, Lee Maltings Complex, Dyke Parade, Cork T12R5CP, Ireland

1.1 Introduction to Vapor Phase Deposition

The basic concept of chemical vapor deposition (CVD) is the growth of a thin solid film by the chemical reactions of a vapor of precursor molecules. These chemical reactions can take place at the surface or in the gas phase, and there are many variants encompassing a wide array of approaches to formulate the film. The basic concept of CVD was first demonstrated in the nineteenth century for carbon and metallic thin films [1–3], and it was further developed for Si [4, 5] and III/V materials [6], but its use in oxides became more widespread after the development of oxide superconductors in the 1980s [7, 8] and the drive for Si integrated circuit technology through scaling of metal-oxide semiconductor field effect transistors (MOSFETs) and dynamic random access memory (DRAM) [9]. In this short review we will briefly introduce the basic concepts of vapor phase growth of metal oxides and selected applications where it has made, or has the potential to make, significant advances in technology.

1.2 Vapor Phase Deposition Methodologies

Common to all vapor deposition systems are a precursor delivery system, a reaction chamber with an energy source to control the chemistry, and an exhaust system where reaction products and excess reagents are safely disposed of. This simplistic description does little justice to the complex engineering solutions that are employed to perform these tasks; however, it is beyond the scope of this article to describe these in detail, and so the reader is directed elsewhere [10, 11]. Many vapor deposition methodologies are used to generate films [10–12], which methods are employed is determined not only by the type of film required but also by the chemical nature and availability of the precursors employed. Here, we will consider two general variants of deposition methods: CVD where reagents are introduced simultaneously

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and atomic layer deposition (ALD) where the reagents introduced are separated by purges. The push for miniaturization in device technology has pushed many traditional CVD processes toward an ALD solution, where material growth is achieved at the atomic layer of precision; however it should be recognized that nanotechnology can still be achieved with traditional CVD methods and that not all materials systems lend themselves to ALD.

1.2.1 Chemical Vapor Deposition

CVD is a complex process that can be described in the form of a schematic (Figure 1.1) where gaseous precursors are introduced into a reactor and through a series of gas phase pyrolysis reactions; partly reacted chemicals diffuse through a boundary layer to interact with a growth surface. Such a description is very much simplified as the growth process is influenced by many parameters that determine the stoichiometry, uniformity, crystallinity, and density of defects of the resultant materials. The consequence of which is that the reactor and chemistry design is extremely complicated and must consider primary and secondary chemistry, mass transport, adsorption, surface diffusion of reactive and exhaust species, and finally nucleation and film densification. The key parameters for growth control are the choice of chemistry, the pressure, and the nature and amount of energy supplied to the system. For a more in-depth treatise on the complexities of reactor design and process control, the reader is referred elsewhere [10].

1.2.2 Atomic Layer Deposition

ALD is a variant of CVD that employs sequential self-limiting chemical reactions at the substrate surface. As illustrated in Figure 1.2, a key aspect of ALD is that the precursors, or their reaction products, do not meet in the gas phase through cyclic pulsing and purging. This cycle of pulses and purges is repeated to build up a thin film of the desired thickness one monolayer per full cycle.

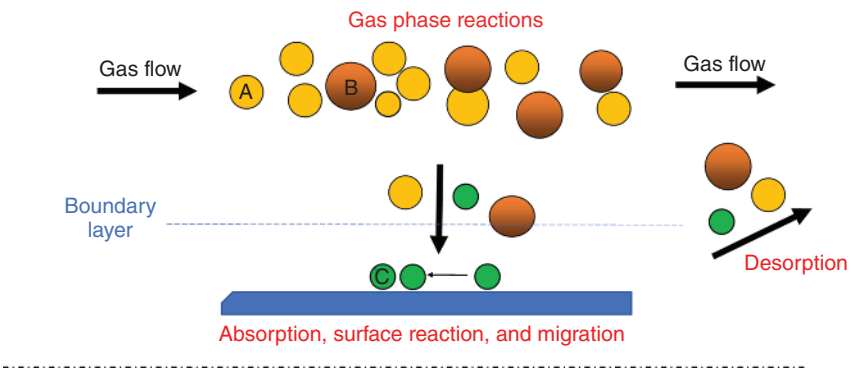

Figure 1.1 Schematic of a generic chemical vapor deposition process. The reagents A and B are transported to the reaction zone, where they undergo a complex range of gas and surface reactions to deposit material C at the growth surface.

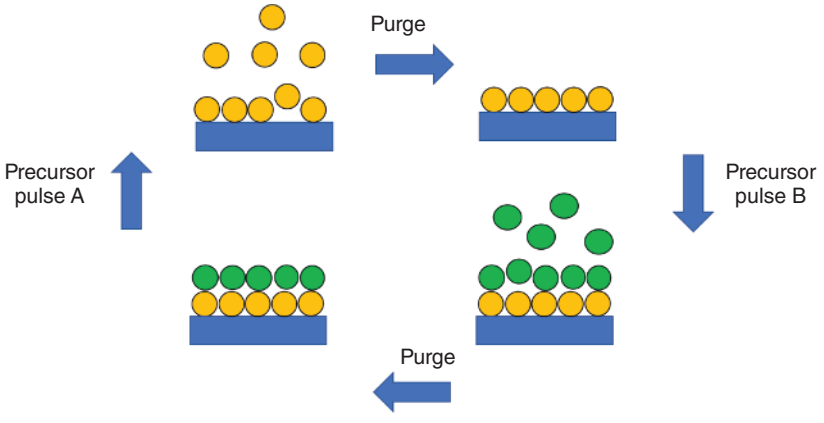

Figure 1.2 Schematic of a typical ALD process. Two precursors A and B react at the surface to produce material AB. The two self-limiting precursor pulses are separated by purges to ensure that excess reactant is removed from the reactor between pulses to prevent gas phase reactions.

In this way the growth can be controlled at the atomic or molecular level. Another key advantage of ALD is that the self-limiting chemistry enables both large area and complex morphologies to be coated uniformly. Self-limiting behavior is a consequence of the precursor only being able to react with functional groups at the substrate surface. Hence, once all the reactive sites have undergone chemical reaction, no further reaction can take place, and excess reagent passes to the exhaust system, the resultant surface remaining in a pseudo-steady state until the co-reagent is pulsed, completing the cycle and regenerating the reactive sites for the next precursor pulse. In addition, the generally low temperature of the ALD process makes it suitable for sensitive substrates, such as polymers and biological samples. The key disadvantage of ALD is the low deposition rates relative to other methods that makes it unsuitable for thicker films. It should also be noted that the low temperature of deposition although advantageous for sensitive substrates can limit the phase selection of materials, with many material systems being limited to amorphous films. The technique of ALD has been extensively reviewed [13–15].

1.3 Precursors and Chemistry

Although the chemistries of variants of CVD are different, the key requirements for the chemical precursors employed are similar. Key aspects are that the precursor is stable under storage and delivery, sufficiently reactive to undergo viable reactions at or near the substrate to produce volatile by-products that can be swept from the reaction zone without contamination of the desired material. Other considerations such as ease and cost of manufacture and any safety implications are also of importance. Generally, precursors are volatile to allow easy transport to the reaction zone; however with the introduction of liquid injection methods, precursors can, in many

cases, be dissolved in a suitable solvent to circumvent volatility issues [11]. The combination of precursors utilized is also vital, the production of materials requiring more than one precursor requires that their reactivity is similar under the chosen reaction conditions to ensure the desired stoichiometry. The choice of precursor used in a specific reaction is often not straightforward and is often determined by the material parameters required as well as the CVD variant being employed [10]. The basic concepts of precursor stability, reactivity, and transportability are determined by the constituent parts of the precursor molecules. ALD precursors need to be volatile enough to be easily pulsed and purged through the reaction zone at temperatures where self-limiting surface chemistry is preserved, but reactive enough so that facile reactions with the surface species and co-reagents are efficient. CVD sources require high stability at evaporation temperatures and clean decomposition at elevated temperatures. These properties are often in conflict; for example, volatility is determined by the intermolecular forces of a source, and this can be improved by increasing the stearic nature of ligands, but this in turn can reduce the reactivity. Thus, what might be a stable, volatile precursor for CVD may not undergo facile reactions with oxygen containing co-reagents that would make it suitable for ALD. Another complication is that trace contaminants that might not be relevant for one application may be seen as catastrophic for others; for example, F substitution of β-diketonates is an excellent method of improving volatility, but F is a serious contaminant, even at low levels, in silicon-based electronics. The chemistry of precursor development for CVD and its variants is complex but is well reviewed elsewhere [10–15].

1.4 Applications of Metal-Oxide Vapor Phase Deposition

Vapor deposition methods are well established and widespread and have been employed to generate metal-oxide-based materials for many application spaces, notably transparent conducting oxides, catalysts, dielectric materials, and protective and decorative coatings. These and many other applications are described in detail in many excellent reviews on the subject [10–15]. In this review, however, due to the wide range of vapor deposition processes and established applications, we will focus on materials and methods, on which our own personal research is centered, namely, dielectric metal oxides, where nanometer scale engineering is essential for realizing many applications. With respect to dielectrics, we will present case studies on two classes of materials: firstly, ferroelectric that displays hysteresis in their electric field response and, secondly, insulating with a linear polarization response to electric field.

1.4.1 Case Study 1: Ferroelectric Oxide Materials

Ferroelectric materials are a subclass of ferroic materials, which also include ferromagnetic and ferroelastic materials. Ferroelectrics are dielectrics that have a net permanent dipole moment due to their polar nature and non-centrosymmetric structure. This spontaneous dipole moment can be switched between two states

using an applied electric field, and a remanent polarization remains when the electric field is removed. All ferroelectrics exhibit pyroelectric and piezoelectric effects, meaning that they can transform thermal energy into electrical energy, and they can create electric charge when mechanically stressed. Ferroelectrics are thus widely used in sensing, actuating, infrared, optoelectronic, surface acoustic wave (SAW), ultrasound, and nonvolatile data storage applications [16].

Oxide ferroelectrics are being pursued due to their diverse properties, their robust performances, and the intriguing phenomena they exhibit. Their structures and compositions can be tuned to control the functionality of the targeted application. Perovskite $KNbO_3$ and ilmenite $LiNbO_3$ have received much attention due to their large piezoelectric constants and electro-optic coefficients (e.g. d_{33} of 121 pC/N for $KNbO_3$ [17] and 6–70 pC/N for $LiNbO_3$, depending on the orientation [18]) and have been used in SAW and electro-optic devices [19]. $LiNbO_3$ has recently emerged as a promising platform for photonic integrated circuits [20]. Piezoelectric, pyroelectric, and electro-optic coefficients can be optimized by forming solid solutions between end-member perovskites. One of the most technologically important and commercially successful ferroelectric systems is the perovskite solid solution system between $PbZrO_3$ and $PbTiO_3$ ($PbZr_xTi_{1-x}O_3$; often referred to as PZT), and excellent properties can be tailored by selecting ceramic compositions in different parts of the phase diagram. Properties can be further improved by partial substitution with selected cations (e.g. *A*-site substitution by Sr^{2+}, La^{3+}, K+, or *B*-site substitution with Sn^{4+}, Nb^{5+}, Ni^{3+}). PZT has been widely used as an active component in microelectromechanical systems (MEMS), actuators, pressure sensors, pyroelectric sensors, medical ultrasound, ultrasonic transducers, and piezoelectric micro-pumps [21, 22].

Layered structured ferroelectrics offer very flexible frameworks for a wide variety of applications, given that differing cations can be accommodated both at the *A*- and *B*-sites. Aurivillius bismuth-based materials are naturally two-dimensional (2D) nanostructured, where $(Bi_2O_2)^{2+}$ fluorite-type layers are interleaved with *m* numbers of perovskite-type units (Figure 1.3). Ferroelectricity arises from polar displacements of cations relative to anions, which stabilizes the polar ground state. This has been exploited for commercial use in ferroelectric random-access memory (Fe-RAM) devices [25, 26, 28]. Recently, it has been shown that ferroelectricity can persist down to thicknesses of only 2.4 nm, which equates to one-half of the normal crystal unit cell, demonstrating that wide-band gap oxide ferroelectrics can be added to the growing class of 2D materials [29]. Room temperature multiferroic (ferroelectric and ferromagnetic) behavior has also been demonstrated [30, 31], offering the prospect of producing eight-state information storage based on simultaneous magnetoresistance and electroresistance [32].

1.4.1.1 Ferroic Thin Films

Thin films of ferroelectric and multiferroic materials are being widely used or are currently being developed for commercial applications including memories, microwave electronic components, and micro-devices with pyroelectric and piezoelectric micro-sensors and actuators [33]. Successful thin film synthesis to satisfy

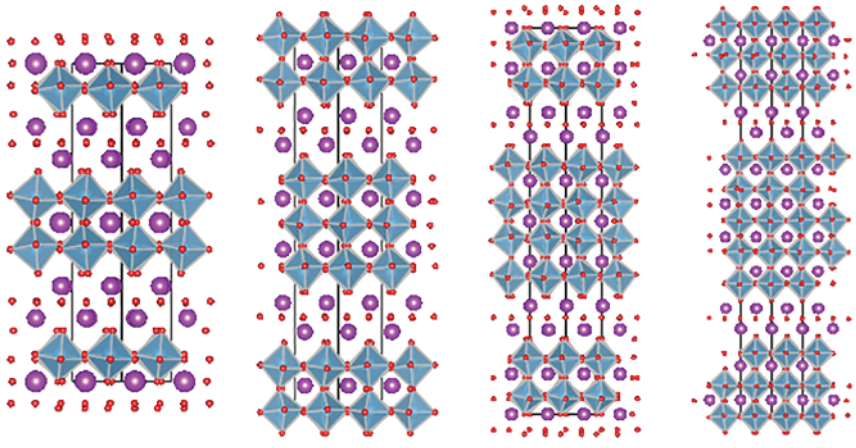

Figure 1.3 Schematics of Aurivillius phase crystal structures projected down the <110> orientation produced using visualization for electronic structural analysis (VESTA) [23] software. (a) $SrBi_2Ta_2O_9$ ($m = 2$; space group *A21am* [24]); (b) $Bi_4Ti_3O_{12}$ ($m = 3$; space group *B1a1* [25]); (c) $Bi_5Ti_3Fe_2O_{15}$ ($m = 4$; space group *A21am* [26]); and (d) $Sr_2Bi_4Ti_5O_{18}$ ($m = 5$; space group *B2eb* [27]). Bismuth or *A*-site atoms are represented by purple spheres; oxygen atoms are represented by smaller red spheres; and BO_6 octahedra are represented by blue polyhedra. Source: (a) Modified from Perez-Mato et al. [24], (b) Modified from Guo et al. [25], (c) Modified from Hervoches et al. [26], (d) Modified from Ismunandar et al. [27].

the requirements of a particular application is demanding [16]. Depending on the targeted technology, it may be necessary that films are uniform, conformal, device compatible, epitaxial, have high orientation control, and are strain controlled. Furthermore, it may be a condition that films are ultrathin, have atomic-level precision, and have atomically sharp interfaces. Aspects to consider during successful processing of the fabricated film into specific device structures may involve integration with heterostructures and multilayers, integration with metallic and conductive oxide electrode layers, integration with silicon, the ability to produce patterned and nano-patterned structures, the use of comparatively low processing temperatures, and the use of reasonably inexpensive processes as well as processes that yield high reproducibility [22].

Over the past three decades, there have been significant improvements in the development of instrumentation and growth processes to enable the synthesis of high quality, reliably produced, and ferroic thin films with technological value. Methods for successful thin film fabrication of piezoelectric, ferroelectric, and multiferroic oxides include chemical solution deposition (CSD) [32], sputter deposition [34], pulsed laser deposition (PLD) [27, 35], ALD [36, 37], molecular beam epitaxy (MBE) [27, 38], and CVD [22, 39]. CVD has been a pioneering method to produce films used in high density nonvolatile Fe-RAM technologies [40]. Within this contribution, we focus on key factors involved in the CVD fabrication of high-quality ferroic thin films. We discuss the specific advantages of the CVD technique toward the growth of ferroic perovskite and layered materials.

Ferroelectrics and multiferroics are often comprised of elements with high volatility such as bismuth or lead. PLD, sputter deposition, and MBE growth techniques operate at relatively low oxygen partial pressures, where issues arising from migration of such volatile elements are intensified. Especially during epitaxial growth, the combination of high crystalline anisotropy and unidirectional growth fronts mean that structural rearrangement is limited to the surface layers of a growing film. As bismuth and lead diffuse out of the films, inadequate activation energies exist to remedy the losses within the film and the structures crystallographically shear to form microstructural defects and secondary impurity phases [41]. Microstructural defects can influence domain wall activity in ferroelectric and ferromagnetic thin films. If defects serve as nucleation sites for reverse domains, coercivity may be decreased. Alternatively, if defects contribute to "pinning effects," these can resist domain wall motion and may lead to increased coercivity [42]. Defects such as oxygen vacancies often lead to degradation of ferroelectric properties, including decreased piezoelectric coefficients and decreased remanent polarization, and can result in increased leakage currents and polarization fatigue [43]. Impurity phases such as non-ferroelectric pyrochlore $Pb_2Ti_2O_7$ and $Bi_2Ti_2O_7$ can also diminish ferroelectric properties [44]. Whereas the presence of ferrimagnetic spinel impurity phases (such as Fe_3O_4 and $CoFe_2O_4$) can complicate the interpretation of an intrinsic magnetic response [45, 46]. Formation of defects and impurity phases can be inhibited by increasing the oxygen partial pressure. However, for techniques such as PLD, sputtering, and MBE, it is often found that this can only be achieved using relatively narrow ranges of deposition conditions. Oxygen loss tends to occur during sputtering deposition of thin film oxides, leading to oxygen vacancy defects and associated ferroelectric fatigue. Furthermore, the use of high-energy particles during deposition can lead to physical damage and defects [47, 48]. Oxygen stoichiometry is a significant issue in MBE, since the ultra-high vacuum conditions (typically 10^{-10} to 10^{-5} Torr) required for MBE growth oppose an oxidizing atmosphere. Accordingly, either molecular or atomic oxygen sources are commonly necessary in MBE to provide sufficient oxygen for growth of thin film oxides [49]. Even so, incomplete metallic oxidation during MBE growth can lead to the formation of oxygen vacancies, n-type conductivity, and electrical leakage issues [50].

Conversely, CVD with its relatively high gas pressure (typically 0.6–70 mbar) and oxygen-rich environments (typically 100–2000 scmm; 5–70% O_2) compared with high vacuum techniques can prevent the re-evaporation of PbO or Bi_2O_3 over wider ranges of growth parameters [22]. Funakubo et al. [51] synthesized epitaxially grown PZT on MgO (100) substrates by CVD over wide deposition conditions (deposition temperature ranged from 600 to 700 °C, with oxygen partial pressures of between 64 Pa and 1.1 kPa and with total gas pressures of between 1.1 and 6.7 kPa). Whereas Pb/(Pb + Zr + Ti) deposition rates notably decreased below oxygen partial pressures of 64 Pa, no significant changes to deposition rates were observed above 64 Pa. The successful preparation of pyrochlore-free, stoichiometric PZT films at lower temperatures and over a wider temperature range compared with sputtering [52] and PLD [53] methods was attributed to the prevented revaporization of

lead under the relatively high total gas and partial gas pressures enabled by this CVD method [51]. Bartasyte et al. [52] employed a pulsed liquid injection organic chemical vapor deposition (MOCVD) technique for the synthesis of $PbTiO_3$ on $SrTiO_3$ (001) and LaO_3 (001) substrates at 650 °C and explored the influence of the oxygen percentage (7%, 15%, 37.5%, and 50%) in the gas flow during deposition. A maximum Pb/(Pb + Ti) ratio and a maximum growth rate were achieved at 37.5% oxygen, due to the promoted formation of PbO compared with lower oxygen concentrations. However, when the oxygen concentration was too high (50%), lead deficient films were achieved. This was explained by the formation of high valency Pb_3O_4 and PbO_2 at higher oxygen partial pressures. By utilizing an increased partial pressure of 0.4 atm oxygen during cooling from high temperatures (800 °C), the lead desorption rate can be reduced. Thus, higher oxygen pressures during cooling stabilize the $PbTiO_3$ phase and enabled an increase in deposition temperature [52]. Dormans et al. [53] report on the organometallic CVD growth kinetics of $PbTiO_3$ on $SrTiO_3$ (001). A PbO partial pressure of at least 10^{-3} mTorr was necessary to form stoichiometric $PbTiO_3$, which was easily achieved by this CVD process. At temperatures of 700 °C and above, the rate of formation of $PbTiO_3$ from PbO and TiO_2 was faster than the rate of desorption of PbO. It was found that a relatively large process window of parameters can be used and stoichiometric $PbTiO_3$ was grown independent of the deposition temperature and ratio of the precursor partial pressures. The growth rate was almost independent of oxygen partial pressure; however, it was noted that the epitaxial quality of the grown $PbTiO_3$ is optimum at an oxygen partial pressure of 2.1 Torr. At higher oxygen partial pressure, it is believed that diffusion of adsorbed species is hindered by adsorbed oxygen, while at low oxygen partial pressures, the films deteriorate due to oxygen deficiency [53].

Furthermore, Micard et al. [54] explain that although good quality $BiFeO_3$ films on IrO_2/Si substrates in terms of structure and composition can be achieved using initial MOCVD parameters (temperatures of 650–750 °C, argon flow of 150 sccm, oxygen flow of 150 sccm, and duration of one hour), it was observed that inclusion of higher oxygen gas flow step had a marked influence on optimizing the film morphology and quality. The initial high oxygen step (900 sccm oxygen gas flow for 10 minutes) encouraged the formation of several $BiFeO_3$ sites, whereas the second growth step (150 sccm for 50 minutes) produced the growth of denser films compared to the previous conditions [54]. Similarly, Tohma et al. [55] report that morphology and grain size of $BaTiO_3$ films prepared on (100)Pt/(100)MgO substrates by MOCVD were influenced by the oxygen partial pressure used during growth, with a maximum grain size of 130 nm achieved at oxygen partial pressure of 66 Pa at deposition temperature of 973 K. The dielectric properties of the $BaTiO_3$ films were in turn influenced by the deposition conditions, with dielectric constant increasing with increasing grain size from 20 to 130 nm.

The ferroelectric and multiferroic properties of complex oxide materials are sensitively affected by their chemical composition. In addition, even slight alterations to composition can lead to abrupt changes to crystal structure and can result in phase transitions between tetragonal and rhombohedral ferroelectric phases across

a morphotropic phase boundary [56]. CSD has the ability to vary stoichiometry in order to discover new phases and to investigate physical properties as a function of composition, using facile and relatively low-cost methods [30, 44, 45, 57]. ALD also enables excellent control over film composition. However, the comparatively low deposition temperatures employed by these techniques tend to produce amorphous films. A subsequent higher temperature post-anneal step is often required for the crystallization of complex oxide phases by CSD and ALD [58]. Progress in the design of CVD process technologies has enabled simple fine-tuning of stoichiometry and reproducibly produced compositions during the direct production of crystalline, epitaxial complex oxide ferroics [59].

Many of the metalorganic precursors available for the growth of ferroelectric and multiferroic oxides are relatively nonvolatile at room temperature, meaning that during conventional CVD, it is necessary to heat the precursors within their bubblers in order to sublime or evaporate the precursors. Not only does this accelerate chemical degradation of the precursors, but it is also often difficult to precisely control the stoichiometry of complex oxide materials during the conventional delivery of low vapor pressure precursors. In 1995, Van Buskirk et al. [60] describe how these issues spurred the use of liquid delivery MOCVD techniques, where multiple liquid metalorganic precursors, even those with low thermal stability and low vapor pressure, are kept at ambient temperature and are maintained under pressure [61]. This allows for the transport of several precursors that can be vaporized instantaneously. Film composition is precisely controlled with process reproducibility by real-time volumetric mixing of the component solutions [60]. Liquid delivery MOCVD studies where the Ba/Sr ratio (70/30) was kept constant, but the Ti flow varied, enabled stoichiometric adjustment of $BaSrTiO_3$ thin films on $Pt/ZrO_2/Si$ substrates. A linear relationship between film composition and precursor concentration was obtained with run-to-run repeatability. The need for stringent process control was illustrated for 90 nm films, where small variations in film composition (approx. 3 Ti at%) yielded a considerable difference (approx. 100%) in dielectric constant. Liquid source MOCVD delivery of high crystalline quality PZT films was also investigated in this work. A wide range of compositions were explored at a deposition temperature of 550 °C, and again a linear relationship between precursor composition and film composition was observed. Measured dielectric constants varied monotonically with composition, with the highest values close to the PZT morphotropic phase boundary [60]. Excellent control of stoichiometry with high compositional uniformity has also been reported for CVD-grown epitaxial $LiNbO_3$ films on $LaTiO_3$ substrates for SAW and optical device applications [59, 62].

The ability to include 5 nm thick Bi_2O_3 buffer layers during liquid delivery MOCVD of $SrBi_2Ta_2O_9$ on $Pt/Ti/SiO_2/Si$ substrates prevents the diffusion of Ti from the substrate and minimizes Bi migration away from the films. In addition to preventing secondary phases at the interface, the bottom Bi_2O_3 buffer layer also acts as a seeding layer, improving the crystallinity of the films $SrBi_2Ta_2O_9$. It was found that the remanent polarization ($2P_r$) of $SrBi_2Ta_2O_9$ samples with a buffer layer ($22.5\,\mu Ccm^{-2}$) significantly improved compared with samples without buffer layers ($14.7\,\mu Ccm^{-2}$) [63]. By increasing the thickness of the MOCVD-grown BiO_x buffer

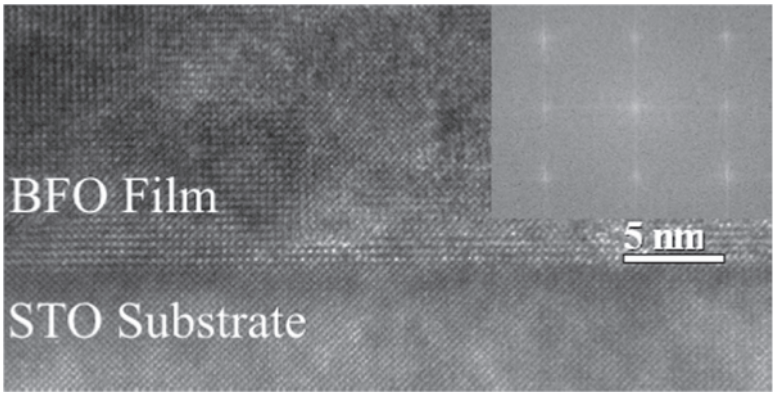

Figure 1.4 A high-resolution transmission electron microscopy (HRTEM) bright field image showing the crystalline nature of the BFO film and a sharp interface with the substrate. The inset image shows the fast Fourier transform of the BFO film obtained from the HRTEM image. Source: Deepak et al. [65]/Reprinted with permission of American Chemical Society.

layer from 5 to 30 nm, it was possible to lower the MOCVD process temperature for 90 nm thick $Bi_4Ti_3O_{12}$ films (on Pt-coated Si substrates) from 550 to 400 °C [64].

Deepak et al. [65] used direct liquid injection chemical vapor deposition (DLI-CVD) to carefully control the concentration of the iron precursor and achieved bismuth self-limiting growth of epitaxial $BiFeO_3$ (BFO) films on $SrTiO_3$ substrates (Figure 1.4). Here, the precursor injection rates were an important parameter controlling stoichiometry. The growth window was defined in this work as the range of relative Bi-to-Fe precursor injection ratios, in which phase pure, stoichiometric BFO films can be prepared. CVD growth of BFO is generally challenged by the volatile nature of bismuth. The growth window is often very narrow, requiring strict control of bismuth volumes and with Bi/Fe precursor injection ratios of between 2.33 and 2.55 [66, 67]. Instead, Deepak et al. [65] exploited the volatile nature of bismuth oxide, to develop a bismuth self-limiting process at a growth temperature of 650 °C, pressure of 10 mbar, and oxygen flow of 1000 sccm (out of a total gas flow of 3000 sccm). Utilizing a significantly higher concentration of volatile Bi and the correct amount of the nonvolatile Fe component, an extension of the CVD growth window was enabled with Bi/Fe ratios of 1.33 to 1.81, without leading to the formation of impurity phases and without the need for stringent control of bismuth injection volumes during growth (Figure 1.4). At the decreased Bi/Fe ratio, the film surface becomes atomically smooth, with a root-mean-square (rms) roughness below 0.4 nm. Figure 1.5a,b demonstrates the amplitude strain butterfly loop and phase loops measured for ultrathin BFO films, respectively. A 180° phase switching can be observed in Figure 1.5b, which is an indication of the retention of ferroelectric switching behavior at sub-10 nm thickness and potential for application in nonvolatile memory storage applications.

Faraz et al. [30] developed DLI-CVD growth processes to synthesize thin films of the complex Aurivillius oxide, $Bi_6Ti_{2.99}Fe_{1.46}Mn_{0.68}O_{18}$. This material system is a rare example of a single-phase room temperature multiferroic to challenge

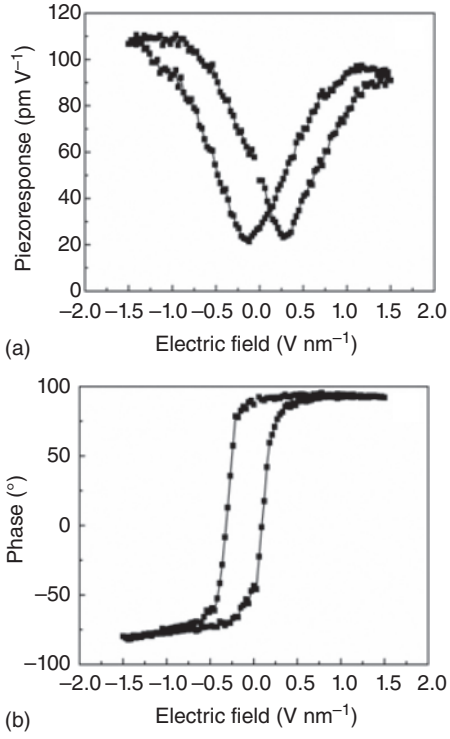

Figure 1.5 Piezoresponse force microscopy (a) amplitude butterfly loop (piezoresponse) and (b) phase hysteresis loop for $BiFeO_3$ thin film deposited on Nb-doped $SrTiO_3$. Source: Reprinted with permission from Deepak et al. [65], Copyright 2015 American Chemical Society.

BFO. Stoichiometric control of manganese is key to ensuring room temperature ferromagnetic behavior [68], and higher magnetization values (M_S 24.25 emu g^{-1}) (Figure 1.6) are achieved using DLI-CVD-grown films compared with CSD-grown films (M_S 0.74 emu g^{-1}) [30].

Increasing levels of integration of ferroic thin films into devices requires the capacity to conformally coat miniature features having challenging aspect ratios at the submicron scales and ultimately at the nanoscale. A chief advantage of CVD over other thin film growth methods is the capability to deposit uniform and conformal thin films of high crystallinity over three-dimensional (3D) structures and within trenches using scalable growth processes. During reaction-rate-limited growth, the deposition rate can be described by the Arrhenius equation [69] with rate constant increasing exponentially with increase in process temperature. Due to the dominating temperature dependence, the deposition rate is only weakly dependent on the homogeneity of precursor flow; therefore, growth in the reaction-rate-limited regime is highly suited to conformal deposition [70].

Burgess et al. [71] demonstrated highly uniform ($3\sigma = 2.25\%$ at 180 nm thickness) planar films of MOCVD-deposited strontium bismuth tantalate and near 100% step-coverage of several patterned structures and recessed features with a 2 : 1 aspect ratio (0.5 μm). Excellent run-to-run reproducibility and conformality of approximately 90% for growth of $SrBi_2Ta_2O_9$ on $Pt/Ti/SiO_2/Si$ on 1 : 1 aspect ratio structures of 0.5–0.6 μm size is also reported [72–74]. By optimizing MOCVD growth conditions, Goux et al. [75] improved the sidewall compositions of $SrBi_2Ta_2O_9$ 3D

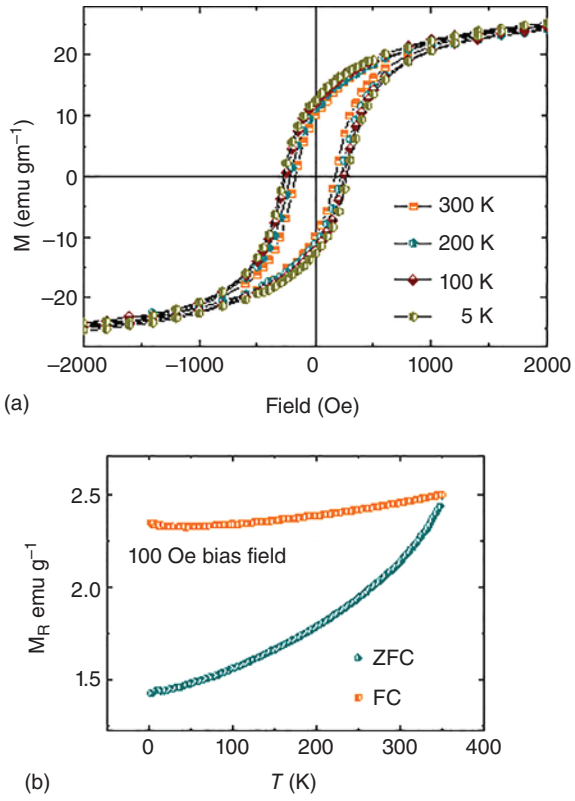

Figure 1.6 (a) Magnetization (M) vs. magnetic field (Oe) of the $Bi_6Ti_{2.99}Fe_{1.46}Mn_{0.55}O_{18}$ sample. (b) Zero field cooled (ZFC) and field cooled (FC) measurements (M_R vs. T). The saturated hysteresis loops and clear split between ZFC-FC curves demonstrate the ferromagnetic nature of the DLI-CVD-grown $Bi_6Ti_{2.99}Fe_{1.46}Mn_{0.55}O_{18}$ at room temperature. Source: With permission from Faraz et al. [30], Copyright 2017 Wiley.

ferroelectric capacitors and decreased the segregation of bismuth impurities and defects at the sidewalls. The ferroelectric contribution of the sidewalls to the overall 3D capacitor was found to be highly contingent on bismuth segregation at the sidewalls. Deposition at 440 °C followed a mass transport-limited regime, where bismuth segregation occurred at nucleation sites at the sidewall due to the increased mobility of bismuth at that temperature. Under these deposition conditions, the sidewall region did not contribute anything to the ferroelectric response and a value of 2.6 μC cm^{-2} was measured for the remanent polarization (P_r) of the 3D capacitor. Optimized growth at 405 °C followed a reaction-rate-limited deposition regime, where bismuth segregation at the sidewalls was reduced. The ferroelectric and leakage properties were notably enhanced, with an increase in sidewall efficiency of up to 50% and P_r for the 3D capacitor increasing to 7.5 μC cm^{-2}.

Close to 100% step-coverage can also be achieved for MOCVD-grown PZT ($PbZr_xTi_{1-x}O_3$) in 3D Ir/PZT/Ir stacks with 2/2 μm (width/distance) trench lines with 1 μm depth (aspect ratio = 0.5) [76]. The PZT films were found to be conformal

on trench lines of these dimensions; however, the step-coverage decreased to 66% for narrower trench lines of width/distance/depth of 0.7/0.7/1 μm. Shin et al. [77] demonstrate how PZT ($PbZr_xTi_{1-x}O_3$, where $x = 0.35$) thin films can be deposited conformally on 3D nanoscale trenches by liquid delivery MOCVD for high density Fe-RAM applications. Almost 100% step-coverage of Ir/PZT/Ir (20/60/20 nm) was obtained for trench capacitors of diameter 250 nm and height of 400 nm. A comparison of trench sizes having differing diameters indicated that the proportion of columnar-type grains increases with increasing trench width. It was observed that trench capacitors having a higher proportion of columnar PZT grains demonstrated superior ferroelectric properties. At 2.1 V, the remanent polarization ($2P_r$) for the 250 nm-diameter trench capacitors was 19 μCcm^{-2}, increasing to 24 μC cm^{-2} for the 320 nm-diameter trench capacitors.

The benefits of conformal CVD growth have been extended to the fabrication of 3D composite magnetoelectric structures. Here, two different materials, one with ferroelectric order and one possessing magnetic order are combined, so when the order parameters couple, polarization can be manipulated by a magnetic field and magnetization can be influenced by an electric field, enabling low-power memories, spintronics, and sensing technologies. Reduced clamping effects from the substrate can be achieved for 3D composites compared with laminate composites, in principle allowing for higher magnetoelectric coupling response. Migita et al. [78] produced microplates of ferroelectric $(Bi_{3.25}Nd_{0.65}Eu_{0.10})Ti_3O_{12}$ (BNEuT) (a-axis orientated) and deposited ferromagnetic $CoFe_2O_4$ (CFO) by MOCVD at 550 °C within the plate gaps with pitches of 5 μm to form composite micro-pillars. The deposition time was varied from 90 to 150 minutes, and a step-coverage of up to 66% was obtained, implying that the deposition progressed via the reaction-rate-limited regime. The CFO structures were single phase with polycrystalline grains, and a preferred orientation along (222) and (511) was reported to promote magnetic anisotropy. For a deposition time of 120 minutes, CFO/BNEuT(h00) composite micro-pillars displayed M_r (remanent magnetization) of 25.7 emu g^{-1} and H_c (magnetic coercivity) of 1.0 kOe. The effect of leakage current was also lowest for this deposition time and ferroelectric hysteresis loops displayed P_r (remanent polarization) of 49 μC cm^{-2} with E_c (electric field) of 264 kV cm^{-1}.

Ultrathin ferroelectrics (typically thinner than 100 nm) are highly desirable due to their technological prospects in data storage applications [59, 79, 80]. For instance, in purely electronic memristors based on tunnel junctions of an ultrathin ferroelectric, the junction resistance sensitively depends on the relative fraction of ferroelectric domains having their polarization pointing toward one or the other electrode. Large on/off ratios between resistance states can be achieved. Furthermore, because ferroelectric switching involves domain nucleation and growth, artificial nano-synapses can be created where synaptic strengths evolve depending on the switching pulse amplitude and duration. This multivalued logic will allow data processing using not only "yes" and "no" but also "either yes or no" or "maybe" operations and thus will serve as unique memory elements in the quest for neuromorphic computing systems [81–83]. A challenge to commercialization is the formation of polarization induced surface charges induced by the out-of-plane polarization which can produce

a depolarization field of magnitude inversely proportional to the dimensions of the ferroelectric [84]. This means that the production of high-quality films, with stable polarization, is essential for effective ferroelectric device performance and reproducibility when scaling down to miniaturized dimensions.

When MOCVD processes follow Frank–Van der Merwe-type growth, in principle it is possible to deposit films in atomic, layer-by-layer deposition modes to achieve films of atomic layer thickness [85]. This is exemplified by $BaTiO_3/SrTiO_3$ superlattices grown epitaxially on $LaAlO_3$ (012) substrates having individual layer thicknesses of 2 nm each (approximately five lattice constants) [86].

Nonumura et al. [87] discuss that for MOCVD growth of ultrathin epitaxial $Pb(ZrTiO)_3$ (PZT) films, the growth mode, film surface flatness, and ferroelectric characteristics are substantially affected by the top surface plane and surface flatness of the underlying substrate. When $SrTiO_3$ substrates were surface treated to a buffered acid etch and anneal, this enabled deposition of $SrRuO_3$ bottom electrodes with uniform terrace ledges. This in turn enabled MOCVD of highly crystalline 20 and 15 nm PZT films by the Stranski–Krastanov growth mode, having sharp and clear substrate–film interfaces and with terrace ledges of similar height to the $SrRuO_3$ terrace ledges. PZT films of 20 nm thick having terrace ledges displayed saturated ferroelectric hysteresis loops (remanent polarizations of 29–33 $\mu C\,cm^{-2}$ and coercive fields of 340–370 $kV\,cm^{-1}$). In contrast, 20 nm thick PZT films without terrace ledges exhibited unsaturated, leaky loops. Ferroelectricity was also observed for the 15 nm PZT films, although large leakage currents at this thickness prevented saturated hysteresis loops.

Fujisawa et al. [88] also used buffered-acid etches and pre-anneals of substrates before MOCVD of epitaxial $PbTiO_3$ films on $SrTiO_3(100)$, La-doped $SrTiO_3(100)$, and $SrRuO_3/SrTiO_3(100)$. High angle annular dark field–scanning transmission electron microscopy (HAADF-STEM) determined an epitaxial relationship and sharp interface between the film and substrate layers and that $PbTiO_3$ films as thin as 1–20 monolayers (0.4–8 nm) were achieved. Contact-resonance piezoresponse force microscopy (CR-PFM) was used to demonstrate piezoelectric response and ferroelectric polarization switching in seven monolayer thick (2.7 nm) $PbTiO_3$ on $SrRuO_3/SrTiO_3(100)$.

It has been emphasized [85] that a critical requirement for future data-storage technologies based on multiferroic materials is the demonstration of room temperature magnetoelectric coupling at the sub-10 nm length scale. Although this is recognized within the multiferroics community as a challenging task, Keeney et al. [89] have made progress in the optimization of multiferroic $Bi_6Ti_xFe_yMn_zO_{18}$ (B6TFMO) toward achieving this goal. Previous films grown on sapphire substrates were approximately 100 nm in thickness and required a post-growth anneal at 850 °C [29, 30]. Optimized, single-step DLI-CVD studies enabled a lowering of the crystallization temperature to 700 °C and epitaxial growth on lattice-matched substrates ($NdGaO_3$ (001), $La_{0.26}Sr_{0.76}Al_{0.61}Ta_{0.37}O_3$ and $SrTiO_3$ (100)). Epitaxial films of thickness 7 and 5 nm were achieved, which equates to 1.5 unit cell and 1 unit cell of the Aurivillius structure, respectively (Figure 1.7). Since there is an enhancement in the diffusion coefficient of bismuth above 710 °C [90], a

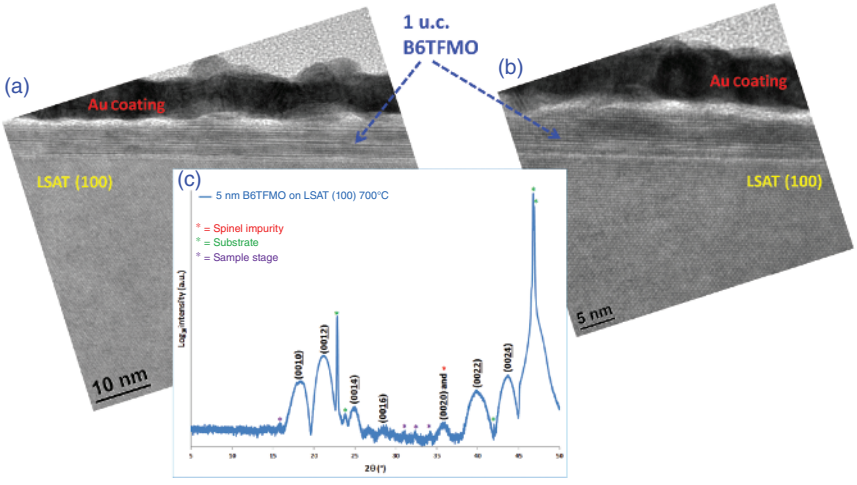

Figure 1.7 (a), (b) Representative TEM images demonstrating continuous 5 nm Aurivillius phase films prepared by the single-step DLI-CVD process (700 °C) on LSAT (100) substrates. (c) Representative XRD pattern demonstrating that the five-layered B6TFMO Aurivillius phase is successfully achieved at 5 nm thickness (1 unit cell (u.c.) thick B6TFMO). This single-step growth process on epitaxial substrates enabled the synthesis temperature of B6TFMO to be lowered by 150 °C. Source: Keeney et al. [89]/Reprinted with permission of American Chemical Society.

lowering of the crystallization temperature by 150 °C decreased the rate of bismuth diffusion and reduced the issues associated with uncompensated stoichiometries and related structural disorder. Film quality, sample purity, and surface roughness (rms = 1.2 nm) were considerably enhanced compared with samples annealed at 850 °C; however a volume fraction of 3–4 vol% spinel magnetic impurities were identified on the film surface, which precluded measurements of magnetic properties intrinsic to the B6TFMO Aurivillius phase. Attention was focused on local ferroelectric measurements of B6TFMO by piezoresponse force microscopy (PFM) where ferroelectricity was confirmed to persist in 5 nm (1 unit cell thick) B6TFMO films, with piezoresponse increasing with increased tensile epitaxial strain. In-plane ferroelectric switching was demonstrated at 1.5 unit cell thickness (Figure 1.8). This work demonstrated that 2D ultrathin B6TFMO films can be synthesized by scalable growth methods, increasing its technological potential for utilization in novel in-plane devices enabling ferroelectric control of tunnel electron resistance. Such in-plane tunnel junction devices would have the significant advantage that performance would not be encumbered by competing depolarization fields upon scaling down to sub-10 nm dimensions.

The layered Aurivillius structures are a technologically important class of materials, demonstrating room temperature ferroelectric and multiferroic properties. Although the layering between bismuth oxide and perovskite blocks occurs naturally during most conventional growth processes, the use of a layer-by-layer growth processes offers the potential for increased control over the layering arrangements and cation site ordering, at temperatures lower than conventional growth processes.

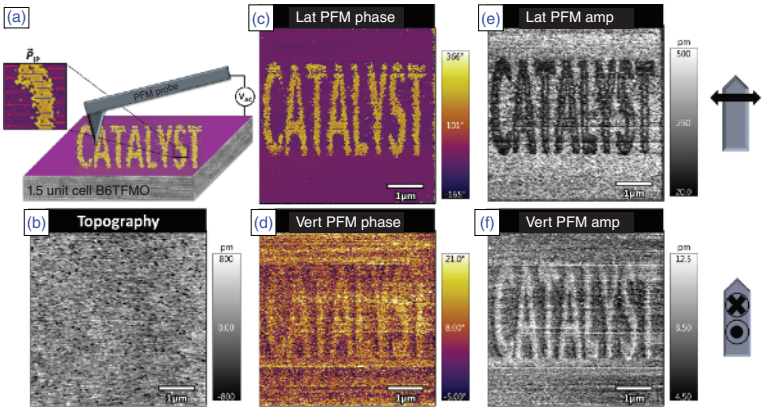

Figure 1.8 PFM lithography studies of 7 nm BTFMO on STO (100) prepared by the one-step process (700 °C). Ferroelectric poling was performed at room temperature with application of +5 V_{DC} (DC bias) to the background and by performing PFM lithography using −5 V_{DC} to write "Catalyst." (a) The "read" step was performed with a probing signal (V_{AC}) of 3.0 V. The red and blue arrows within a close-up of a switched area represent the direction of the in-plane polarization (P_{IP}). (b) Unchanged sample topography after the ferroelectric poling step. (c) Lateral (Lat) PFM phase, (e) lateral PFM amplitude (amp), (d) vertical (vert) PFM phase, and (f) vertical PFM amplitude images. The direction of motion of the PFM cantilever as it scans the sample surface is indicated to the right of the figure. These studies demonstrate the stable in-plane ferroelectric switching behavior for 1.5 u.c. thick B6TFMO. Source: Keeney et al. [89]/Reprinted with permission of American Chemical Society.

Layer-by-layer deposition by ALD has proved highly successful for the growth of ferroelectric $Hf_{0.8}Zr_{0.2}O_2$ films on Si at temperatures as low as 250 °C [36, 80]. However, an extra post-anneal step is required to crystallize Aurivillius films deposited by ALD [58], whereupon the additional heat energy can alter the rearrangement of the deposited layers. Alternatively, layer-by-layer deposition using DLI-CVD enables the possible formation of multilayers and graded composition layers in addition to complex-layered oxide materials [22].

Deepak et al. [91] used a single-step, layer-by-layer, or sequenced DLI-CVD process to synthesize epitaxial ferroelectric $Bi_4Ti_3O_{12}$ films on $SrTiO_3$ (001) substrates with greater control over processing conditions and at temperatures as low as 650 °C. As opposed to simultaneous pulsing of the two liquid precursors, this layer-by-layer growth process was made possible by alternating the number of pulses of bismuth and titanium to mimic the layered Aurivillius phase structure long the *c*-axis. Bismuth and titanium concentrations were controlled by regulating the opening time of computer-operated injectors. The time gap between one set of pulses was kept constant at five seconds, with the total set signifying one loop, corresponding to one half of a $Bi_4Ti_3O_{12}$ unit cell. This loop was cycled 20 times to achieve films of approximately 33 nm thickness, which is equivalent to the thickness of 10 unit cells of $Bi_4Ti_3O_{12}$. The films were relatively smooth, with rms roughness of 1.4 nm. The effect of varied bismuth and titanium concentrations on $Bi_4Ti_3O_{12}$ growth was investigated, and it was found that departures from stoichiometry affected film crystallinity and encouraged the presence of out-of-phase boundary

(OPB) defects. Interestingly, it was determined that the OPB defects did not form due to reasons of bismuth migration and their presence was associated with atomic rearrangements that gave rise to an increased crystalline quality of the films [91].

This sequential, layer-by-layer growth method was extended to include iron within the Aurivillius structure, to expand its applicability toward multiferroic materials [92]. The preciseness of the liquid precursor injection system allowed insertion of monolayers of titanium oxide and iron oxide into the Aurivillius structure to investigate the growth mechanisms for $Bi_4Ti_3O_{12}$ ($m = 3$) and $Bi_5Ti_3FeO_{15}$ ($m = 4$). Structural changes as a function of miniscule variations in precursor concentrations were investigated, and it was observed that the growth mode shifts from Stranski–Krastanov growth mode to layer-by-layer (Frank–Van der Merwe) growth mode as the composition changes from $Bi_4Ti_3O_{12}$ to $Bi_5Ti_3FeO_{15}$. When the concentration of iron precursor was lower (Ti:Fe ratio of 3 : 0.3) than that required to insert a full half unit cell ($m = 3.5$) or full unit cell ($m = 4$) into the Aurivillius structure uniformly over the entire film, the only way to accommodate the extra iron and to maintain charge balance between differently charged Fe^{3+} and Ti^{4+} was to accommodate small regions of the four-layered Aurivillius structure, accompanied by OPB defects. As the iron concentration was increased (e.g. Ti:Fe ratio of 3 : 0.57), there was an increase in the random stacking of $m = 4$ layers between $m = 3$ layers and an increase in c-axis lattice parameter (Figure 1.9) until the pure, smooth (rms roughness < 0.5 nm) epitaxial $m = 4$ composition was achieved at a Ti:Fe ratio of 3 : 1.2. A precise control over structural order was demonstrated, and no bismuth oxide impurity phases were observed in this bismuth self-limiting growth method [92].

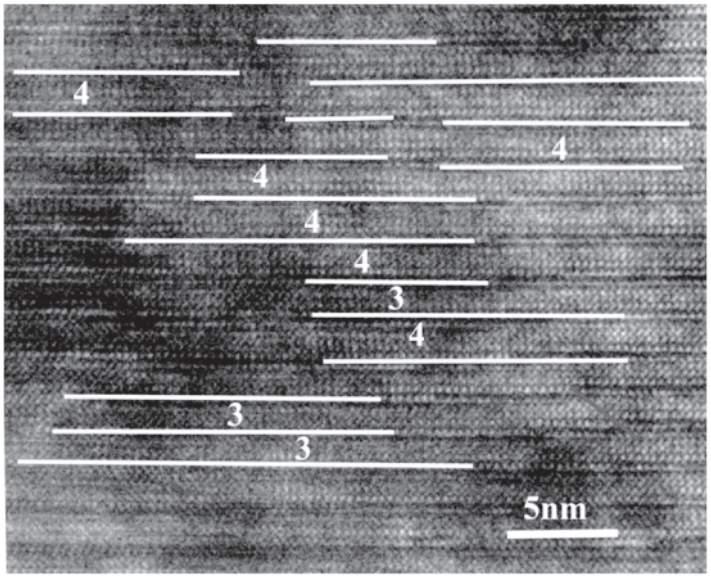

Figure 1.9 The high resolution TEM image of the Aurivillius phase film with Ti/Fe ratio 3/0.57. Source: Deepak et al. [92]/Royal Society of Chemistry/CC BY 3.0.

The preceding sections describe how CVD is flexible and versatile, yet simple and robust and is highly compatible for the production of complex oxide ferroic thin films of technological relevance, with quality approaching that of compound semiconductor films. Specific advantages of the CVD technique toward the growth of ferroic perovskite and layered materials include relatively high gas pressures, stoichiometric control, conformal growth, and ability to produce ultrathin films and layer-by-layer growth processes. In addition, the well-understood tool design with comparatively low cost of ownership and a shower-head design allowing scalability to large wafer sizes (>300 mm) makes CVD particularly amenable to industrial processes [40].

Competitive wafer throughputs (typical deposition rates of 30 Å in 20 seconds) [93] can be obtained without compromising stoichiometry and uniformity control. Furthermore, thermal plasma spray CVD, with its relatively high deposition rate of 0.1 μm min^{-1} and large area deposition (>5 in. diameter), has shown to be an effective method for the deposition of epitaxial $LiNbO_3$ films for optoelectronic device applications, typically requiring thickness of 1–100 μm [94].

Development of more cost-effective precursors is continuing and Moniz et al, [95] created a comparatively low-cost, solution-based aerosol-assisted CVD process for $BiFeO_3$ thin films using a relatively nonvolatile single-source precursor, $[CpFe(CO)_2BiCl_2]$ (Cp = cyclopentadienyl, C_5H_5) dissolved in tetrahydrofuran. Deposition was enabled at temperatures as low as 300 °C; however a post-deposition anneal treatment at 700 °C was required to crystallize phase pure $BiFeO_3$ films.

As miniaturization of electronic devices continues, the need for a high degree of film thickness conformality over complex device topographies will become even more important. As outlined in a recent review by Abelson and Girolami [96], various strategies exist to improve the conformality of CVD processes, including the use of growth inhibitors, the use of two co-reactants to allow a kinetic regime in which the growth is inherently super-conformal, and the use of forward-directed flux depositions.

1.4.2 Case Study 2: Dielectric Oxide Materials

A passive dielectric material is an insulator in which, under an applied electric field, the charges associated with the atoms are polarized and relax when the field is removed. Although such dielectric metal oxides have been used in a wide range of applications, notably stable high efficiency energy storage devices [97–100], here we focus on the requirements for high-quality dielectric material as driven by advances in the miniaturization of integrated circuits and the subsequent need to replace SiO_2 as the gate oxide in the MOSFET. For 30 years SiO_2 was considered an ideal dielectric for this role, easy to fabricate through simple thermal processing, inert, surface pacifying, and exhibiting very few electronic defects. However, the continual scaling of device dimensions reaches a limit where the tunnelling current through the SiO_2 is too great for effective device operation. Equation (1.1) describes the capacitive behavior of a dielectric material of dimensions A and t, where ε_0 is

the permittivity of free space, k is the relative permittivity (dielectric constant), A is the device area, and t the dielectric thickness:

$$C = \varepsilon_0 \, kA/t \tag{1.1}$$

From Eq. (1.1) it can be seen that to maintain the capacitance and to prevent tunnelling in a shrinking device, the dielectric material thickness and permittivity both need to increase. For comparative purposes, thickness of a high k is often referred to as the effective oxide thickness (EOT) that is equivalent to SiO_2 using Eq. (1.2):

$$\mathrm{EOT} = \left(\frac{k_{\mathrm{SiO_2}}}{k_{\mathrm{High-k}}} \right) t_{\mathrm{High}-k} \tag{1.2}$$

As the k value of SiO_2 is ~3.7, there are a whole raft of materials that could be potential replacements. However, requirements for this material system are stringent; the material would need a large band offset to silicon, generate a good electrical interface, must be stable at processing temperatures, and exhibit few bulk defects, and, furthermore, to be commercially viable, it would also need to enable several generations of scaling. Many candidate systems were identified: Al_2O_3, HfO_2, ZrO_2, TiO_2, Ta_2O_5, La_2O_3, and several multicomponent oxides. The band gaps of the common alternative oxides and their k values are presented in Table 1.1.

Although possessing only a moderate k value, Al_2O_3 has been developed as a short-term solution to scaling as it has an amorphous nature, even under robust processing conditions, and has excellent thermodynamic stability at the silicon interface. Aluminum trihalides were widely used in both hydrolysis and oxidation reactions for the CVD of Al_2O_3 [14, 104, 105]; however the high growth temperatures (700–900 °C) are not ideal for microelectronics applications as at these growth temperatures Al will diffuse into the semiconductor material. Lower temperature processes were achieved with several alternative precursors, notably aluminum alkoxides and aluminum alkyls [106]. Although high-quality films were achieved with both precursor groups, the high stability and reactivity of trimethylaluminum (TMA) made it an ideal precursor, enabling high-quality CVD at 400–700 °C and ALD at <250 °C [14, 107–109], well within the thermal restrictions of CMOS processing. Although the pyrophoric nature of TMA is of concern for safety, a viable

Table 1.1 Band gaps and k values of alternative dielectric oxides.

Composition	k value	Band gap	References
Al_2O_3	9	8.8	[101]
HfO_2	25	5.8	[101]
ZrO_2	29	5.8	[101]
TiO_2	25–85	3.2	[101]
$HfSiO_4$	15–17	6.5	[102]
La_2O_3	30	6	[103]
Ta_2O_5	26	4.4	[103]

alternative source has not yet been fully realized, and hence it is still the go-to source for the CVD and ALD of aluminum containing thin films [108].

Although there are a wide range of MOCVD and ALD processes for the growth of La_2O_3 films, their chemistry is not simple and yields films of variable quality [11]. More significantly La_2O_3 is not widely employed in logic devices as it tends to promote large negative flat band shifts in the capacitance voltage responses of MOS devices, hence affecting their operating voltage [109]; also, the moisture-sensitive nature renders La_2O_3 unsuitable for very large-scale integration (VLSI) processes as these involve frequent exposure to atmosphere.

The high thermal stability and dielectric constant of Ta_2O_5 coupled with its low leakage and high breakdown voltage have made it a subject of extensive research particularly in memory and off-chip capacitors devices [110]. More recently Ta_2O_5 has emerged as a leading candidate in memristor technology where ALD films as thin as 1–2 nm have exhibited resistive switching properties [111]. Controlling the defective nature and stoichiometry of tantalum oxides in conjunction with careful selection of electrode materials was found to strongly influence the performance of the resistive switching memory devices [112]. Furthermore, the introduction of composite oxide materials such as ZrO_2–Ta_2O_5 have also renewed interest [113, 114].

As dielectric materials, ZrO_2 and HfO_2 were deemed excellent candidates, due to their high dielectric constants and near-ideal band gaps and offsets to silicon [103], the oxides of Zr and Hf have three structural phases – monoclinic (space group $P2_1/c$), tetragonal ($P4_2/nmc$), and cubic ($Fm3m$) – with either amorphous or monoclinic materials being the dominant as-grown material phase [115]. The CVD and ALD of ZrO_2 were widely reported; MOCVD using the chlorides $ZrCl_4$ [116] and $HfCl_4$ [117] for ZrO_2 and HfO_2, respectively, was found to be complex, due to the low volatility of the sources and need for growth temperatures in excess of 800 °C. However, for ALD processes the high decomposition temperature of halide sources is an advantage as surface-driven reactions occur at much lower temperatures leading to lower particle formation and excellent self-limiting chemistry [118, 119]. For MOCVD a range of β-diketonates compounds were demonstrated. The β-diketonate pentane-2,4-dionate (acac) was found to produce films with very high levels of carbon contamination for both $[Zr(acac)_4]$ and $[Hf(acac)_4]$. However, other β-diketonates were found to deposit high-quality films, $[Zr(thd)_4]$, where thd = 2,2,6,6-tetramethylheptane-3,5-dionate; despite its low volatility and high deposition temperature (>600 °C), was one such source. The issue of low volatility of β-diketonates was addressed by differing methods; the substitution of F for H in the complexes improved volatility, but the presence of F was of concern to device manufacturers [120]. An alternative approach was to change the precursor delivery system to liquid injection using a volatile but unreactive solvent; by this method 2,7,7-trimethyl-3,5-octanedionate (tod) was employed in both $[Hf(tod)_4]$ and $[Zr(tod)_4]$ to grow at lower temperatures and higher growth rates than the thd β-diketonate [121]. The use of alkoxides in MOCVD has been widespread despite complications due to the formation of dimers and polymers reducing the volatility of the sources [122]. The monomeric *tert*-butoxide $[(OBu^t)]$ group has been used in both ZrO_2 $[Zr(OBu^t)_4]$ and HfO_2 $[Hf(OBu^t)_4]$ deposition

by MOCVD [123, 124]. In the case of ALD, despite high-quality films, the process was found to be not self-limiting, due to a surface β-elimination decomposition pathway being open to the [(OBu^t)] group [125]; consequently, it was not deemed suitable for device applications where uniformity of growth at high aspect ratios is often required. To suppress the oligomerization of alkoxides, bidentate species were added to create heteroleptic complexes that often combined the favorable properties of the differing ligands. For example, the addition of β-diketonates metal alkoxides to form a series of compounds [$Zr(OBu^t)_{4-x}(acac)_x$], where $x = 1–3$, greatly improved MOCVD process control and deposition rate [126]. The addition of a range of neutral donor functions into alkoxides produced significant advances in their viability as sources for the MOCVD of HfO_2 and ZrO_2, of note was the ligand mmp (1-methoxy-2-methyl-2-propanolate), which when used independently or in conjunction with the *tert*-butoxide group, for example, [$Zr(mmp)_4$] and [$Zr(OBu^t)_2(mmp)_2$], in liquid injection MOCVD produced capacitive structures for both metal oxides on silicon that demonstrated accumulation, depletion, and inversion (at 100 kHz). Furthermore, trapped charge and flat band shifts in the CV response were relatively small [127]. The use of the neutral donor functions in alkoxide precursors for ZrO_2 and HfO_2 ALD also produced good quality material; however, the absence of self-limiting growth was still evident [128–130].

Metal alkylamides are well-established Hf and Zr precursors for MOCVD with both [$Zr(NEt_2)_4$] and [$Hf(NEt_2)_4$] generating stoichiometric films with low levels of impurities [131, 132]. For these alkylamides, it is ALD where they have shown the greatest impact, not only maintaining the low impurity levels but also demonstrating self-limiting growth across a significant temperature window, with low impurity levels detected in the grown films [133–137]. For Hf and Zr the dimethyl, diethyl, and ethyl methyl amines have been successfully employed with ALD windows of 100–300 °C and growth rates of ∼0.1 nm per cycle. Recently the dimethylamine-based precursor has become dominant, due to a higher vapor pressure and ease of carrier transport. It should be noted that many other sources have been tried in both ALD and CVD, including cyclopentadienyls [138, 139] and hydroxylamides [140]; however, despite showing promise under specific conditions, these sources have not been widely adopted, commercially or in the research community, due to either process complexities or a short fall in materials properties.

Although similar to ZrO_2 in many aspects, HfO_2 became the dominant choice as an insulating dielectric in microelectronics due to its enhanced stability at the silicon interface, leading to little or no formation of interfacial silicates [141] as opposed to ZrO_2 where distinct amorphous zirconium silicates were generated [142]. The greater thermodynamic stability of HfO_2 with Si under processing conditions, such as the 1000 °C anneal required to activate source and drain dopants, is vital as the formation of a lower k interface between the semiconductor and dielectric can seriously impinge on the overall EOT of the dielectric, in addition to creating charge traps in the semiconductor band gap [103]. Significantly, CVD HfO_2-based high-k dielectrics were introduced into the gate stack of MOSFETs at the 45 nm technology node [143].

As scaling progressed further, the search for a semiconductor replacement for silicon intensified. III/V materials had long been considered potential alternatives to silicon-based transistors due to their enhanced electron transport properties; however progress was slow relative to the successful scaling of silicon-based devices with early research moving away from vapor phase processes. The first III/V device was fabricated in 1967 based on SiO_2–GaAs [144]; however the limits of low *k* materials remained. This development of alternative semiconductor materials refocused research in dielectric materials. However, in contrast to the rapid development of Si/SiO_2-based MOSFETs, based on simply scaling transistor design, considerably less progress has been made in the performance of the III/V transistor. Although the early gains were obtained largely with physical vapor deposition methods, high performance inversion mode III/V MOSFETs with InGaAs channel were eventually demonstrated using the vapor phase method of ALD, using high-*k* dielectrics such as Al_2O_3 [145], HfO_2 [146], HfAlO [147], and ZrO_2 [148]. These advances were significant as CVD methods, despite their difficulties are a preferred commercial technology due to their demonstrable scalability. However, with CVD processes, issues with native oxides are exacerbated by the higher-pressure regime employed, as III/V surfaces readily react with atmospheric gases to form native oxides. Surface layer oxides for the $In_{0.53}Ga_{0.47}As$ system generally exist in stable oxidation states of +5, +3, and +1 and small amounts of metallic As–As [149] with stable $In_{0.53}Ga_{0.47}As$ oxides thought to include As_2O_3, As_2O_5, Ga_2O_3, Ga_2O, In_2O_3, $GaAsO_4$, and $InAsO_4$ [150]. Arsenic oxides have been determined to be the least stable oxides in the system, while Ga oxides the most stable [151]. GaAs systems have similar native oxides present, lacking the contribution from indium compounds and dimers, mainly consisting of As_2O_3, As_2O_5, Ga_2O_3, and Ga_2O in addition to a small amount of elemental As [152]. The native oxide of InP has largely been shown to consist of $InPO_4$ and In_2O_3 with In, P, P_2O_3, and P_2O_5 [153, 154]. Antinomy-based III/Vs are increasing being considered for electronics applications [155]; the stability of antinomy oxides that could be formed at the interfaces has been determined by density functional theory [156].

The poor electrical quality of these mixed native oxides leads to poor devices with sub-optimal performance and high levels of device failure. Hence, to utilize vapor phase growth methodologies, these oxides need to be removed or improved in quality [157]. A wide number of studies have been performed using an array of techniques for both binary and tertiary III/V materials. These include chemical pretreatments with HF [156], NH_4OH [158], or sulfides [159–165], thermal treatment methods [166–168], capping layers [169], plasma treatment [170], and combinations of these treatments [171]. Although not all successful, significant progress was made through the use of these surface treatment methods in conjunction with vapor phase deposition techniques, notably surface passivation by the use of sulfides. The use of sulfide treatments has taken several approaches; of these wet chemical methods are the most commonly employed, and of these ammonium sulfide solution, $(NH_4)_2S$, the most widespread, where a range of concentrations, exposure times, and temperatures, has been explored. For example, Peralagu et al. [165] examined $GaSb/Al_2O_3$ MOS structures applying an aqueous $(NH_4)_2S$ pretreatment prior to ALD growth of 8 nm of Al_2O_3. The growth process

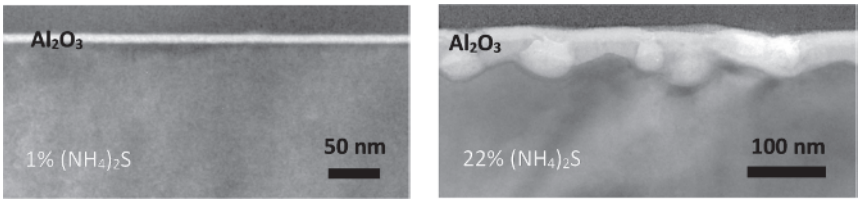

Figure 1.10 Cross-sectional TEM micrographs of (a) 1% and (b) 22% $(NH_4)_2S$ on GaSb showing that the pre-growth etch characteristics have a significant influence on the ALD growth of oxides on II/V materials. The increased surface roughness and resulting interfacial layer are clearly evident. Source: Peralagu et al. [165]/with permission of AIP Publishing LLC.

was performed at 300 °C with TMA and water with a sub-four-minute transfer time between solution processing and reactor sample loading. Peralagu et al. studied devices with the interfaces treated with 1%, 5%, 10%, and 22% $(NH_4)_2S$ solution concentrations at 295 K. Capacitance–voltage (CV) measurements of the MOS devices obtained with the 1% solution exhibited the smallest stretch-out and flat band voltage shifts, and they also demonstrated the largest capacitance swing. Transmission electron microscopy revealed the formation of interfacial layers and increased roughness at the Al_2O_3/*p*-GaSb interface of samples treated with the higher $(NH_4)_2S$ concentration solution (22%), Figure 1.10. It should be noted that such an observation highlights that $(NH_4)_2S$, in addition to passivation, significantly etches III/V materials with the rate of etch being dependent on the III/V material in question; for example, a 10% solution of $(NH_4)_2S$ on GaSb significantly degrades the semiconductor and the interface with the dielectric, whereas for $In_{0.53}Ga_{0.47}As$ it is widely believed to exhibit the best interfacial properties after such an etch. O'Connor et al. demonstrated through multifrequency CV analysis a minority carrier response in both n-type and p-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ devices after such a treatment [171].

Although improvements in performance due to sulfur passivation was clear from many studies, the efficacy of processes were seen to be highly variable. Hurley et al. [172] observed that although the conditions of the passivation by $(NH_4)_2S$ were important, the key determinant of electrical performance was the length of exposure to atmosphere, between the wet chemical etching and the isolation from atmosphere in the ALD growth chamber. As illustrated in Figure 1.11, Hurley et al., employing multifrequency CV measurements on identically grown $InGaAs/Al_2O_3$ MOS structures, found that inversion was only observed if the air exposure was three minutes or less [172].

A potential solution to the short-lived passivation by sulfides was investigated by O'Connor et al., employing passivation of $In_{0.53}Ga_{0.47}As$ with H_2S in situ to a metal–organic vapor phase epitaxy (MOVPE) reactor prior to transfer to an ALD reactor. H_2S was found to passivate the surface in a similar manner to $(NH_4)_2S$, improving performance and suppressing the formation of arsenic oxides; however due to a short air-break between reactors, true inversion was not observed [160].

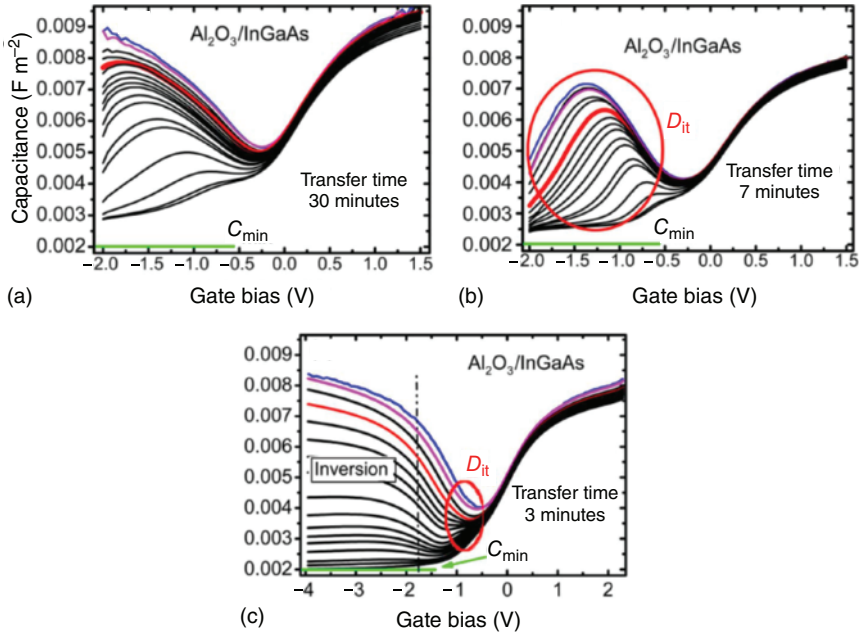

Figure 1.11 Room temperature multifrequency $C-V$ responses for Al_2O_3(8 nm)/$n-In_{0.53}Ga_{0.47}As$/InP MOS structures with Au/Ni gates. The $In_{0.53}Ga_{0.47}As$ surface experienced a 10% $(NH_4)_2S$ surface preparation. Results are shown for varying transfer times from the 10% $(NH_4)_2S$ solution to the ALD reactor of (a) 30 minutes, (b) 7 minutes, and (c) 3 minutes. The samples illustrate the effect of a progressive reduction of D_{it} and the emergence of surface inversion for the case of the 3-minute transfer time in Figure 1.9(c). Source: Hurley et al. [172]/with permission of IEEE.

Although surface treatments made significant improvements to the high k semiconductor interface, it was the growth of high-quality interface materials by ALD, often combined with surface treatments, that have made the biggest advance in electronic properties. The use of ALD was itself determined to remove surface oxides through a self-cleaning mechanism during the deposition process. This self-cleaning mechanism was influenced by the precursor and dielectric choice; consequently, the best performance characteristics of the logic devices was not determined by the dielectric's k value but the interface quality [157]. The first report of this self-cleaning by ALD was by Ye et al. [173], where a thinning of the native oxides of GaAs to 0.6 nm was observed after the ALD of Al_2O_3, with a corresponding reduction in the density of interface defect states (D_{it}) to $\sim 10^{12}\,cm^{-2}eV^{-1}$. Frank et al. [174] also demonstrated the reduction of GaAs native oxides from 2.5 to 1 nm upon deposition of 4 nm of Al_2O_3. The nature of these processes for both Al_2O_3 and HfO_2 ALD were further illustrated by Brennan et al. [135], Lee et al. [175], and Milojevic et al. [176] who all reported that the initial metal precursor pulse, on GaAs and InGaAs substrates, is responsible for the majority of arsenic oxide removal with subsequent metal precursor pulses being required to minimize the presence of gallium oxides. More detailed X-ray photoelectron spectroscopy (XPS) investigations by Hinkle et al. confirmed

that the metal precursor pulse removes native oxides with no reoxidation of the semiconductor surface with the subsequent oxygen containing precursor pulses. It was also revealed from this XPS study that an initial pulse of trimethylaluminum provided a reduction in the +3 surface states, whereas the TDMAH precursor provided a reduction in +5 native oxides present. This observation led to the postulation that cleanup reactions are precursor oxidation state dependent [177].

The mechanistic details for these self-cleaning reactions have been modeled; for Al_2O_3, Klejna et al. [178] postulated that a ligand exchange process was dominant, whereby for trimethyl aluminum, the Al^{3+} preferentially replaces arsenic and gallium oxides in the 3+ oxidation state, resulting in AlO_x formation and $As(CH_3)_3$ and $Ga(CH_3)_3$ as volatile reaction products. Likewise, ligand exchange was proposed to explain the removal of As—O bonds with the accompanying production of volatile elemental arsenic (As_4). More recently investigations of precursor dosing suggest that self-cleaning and interface modification occurs during the first two cycles of Al_2O_3 deposition with bulk film growth dominating after this [179]. Similarly, Suzuki et al. indicated that an interface control layer of 0.2 nm thickness may provide the same benefit as thicker depositions when seeking to improve the dielectric–semiconductor interface [180].

The self-cleaning mechanism for HfO_2 precursors is less well understood, the +4 oxidation of the Hf precursor provides no energetically favorable direct ligand exchange with either the +3 or +5 native oxides, implying that the prevalent cleanup reaction must take place by another mechanism. Furthermore, there are several conflicting reports of the efficacy of the process with tetrakis(dimethylamido)hafnium (TDMAHf); Shahrjerdi et al. [180] reported that no self-cleaning takes places on GaAs at 200 °C. Later Hackley et al. [181] reported interfacial oxide cleanup taking place at 275 °C, and Suri et al. [182] reported that TDMAHf requires a deposition temperature of at least 300 °C to achieve an interface almost completely free from oxides. It was suggested that this was due to the partial decomposition of TDMAHf, whereby Hf loses one out of four Hf–N linkages at 275 °C and two Hf–N linkages at 355 °C, hence cleanup reactions are facilitated by reactive intermediate species [183]. More recently, McDonnell et al. [184] reported the interface cleaning with TDMAHf at 200 °C, and after a NH_4OH pretreatment etch, they attributed the differences in their observations to those of previous measurements to reoxidation of samples due the ex situ nature of the prior studies. Despite the self-cleaning mechanisms of ALD not being fully understood, it has emerged as a widely used method for device optimization, coupled with sub-nanometer thickness control of ALD and the development of interface control layers where materials having not particularly high k, but with excellent stability and low interface defects, have paired with higher k materials to give a sufficiently high EOT values. For example, O'Mahony et al. employed thin films of either MgO and Al_2O_3 as interface control layers between the semiconductor and high k material, to counter poor interfacial properties of HfO_2 and ZrO_2 with $In_{0.53}Ga_{0.47}As$ while maintaining a sufficiently high EOT value [185].

The drive for further scaling of complementary metal oxide semiconductor (CMOS), both in terms of physical dimension and power consumption, has created interest in replacing the channel materials with graphene and other 2D materials,

for which it has been suggested that nanometer scale layers can still provide the carrier transport requirements for logic devices [186]. Current technology does not permit an all-2D material solution for device fabrication; thus the ALD of metal oxides appears to be an ideal method to enable integration of these materials; the low temperature and surface-controlled growth mechanisms of ALD enable low damage and smooth and conformal growth [15, 187]. However, 2D materials by their very nature have no out-of-plane bonding and rely on defects, dangling bonds, to initiate growth. Consequently, the higher the quality of the 2D material, the lower incidence of defects available for nucleation. The low level of active bonding sites promoted non uniform growth with selective growth along grain boundaries and step edges [188–190]. To counter this interface modification and surface activation were once again key in the vapor phase growth of dielectrics on semiconducting layers [187, 190]. The first 2D material studied was graphene, and initial studies used highly ordered pyrolytic graphite (HOPG) as a model substrate due to its ease of production and graphene-like surface with sp2 bonded carbon on terraces and defects at the step edges [191]. Uniform films of Al_2O_3 were produced on HOPG by dosing with NO_2 [192], a method that was previously employed in the ALD coating of carbon nanotubes [193]. An alternative approach was to functionalize the HOPG via a solution process prior to ALD [194]. The most widespread solution however was to replace the traditional ALD co-reagent H_2O with the more reactive species O_3 [195–199]. This approach was tuned, through temperature and O_3 concentration, to prevent the formation of surface species such as epoxide, carbonyl, and carboxylic groups, which would be detrimental to the electronic properties, with the O_3 only being physisorbed to the graphitic surface [196, 197]. The extension of these methodologies from HOPG to graphene was not always straightforward; the ultrathin 2D nature of graphene allows significant substrate effects through the 2D material to growth interface. Unlike HOPG the underlying substrate is usually a different material; for example, graphene is often grown on a catalytic metal surface [198], or flakes are transferred from a bulk sample, potentially leaving residue. Such factors can have a significant influence on the surface chemistry and subsequent grow processes for dielectric layers [199]. Although the methods used for the vapor deposition on HOPG were employed with some degree of success, more controllable methods were deemed necessary. Methodologies to physisorb oxygen entities to promote ALD nucleation were widely studied, employing either O_3 or O_2 plasma, and it was demonstrated that by careful control of the energy of the system, these physisorbed species could initiate growth without damaging the graphene [200–203]. Chemical functionalization, with organic molecules forming π–π interactions with graphene and reactive function groups for binding to the ALD precursor, were also found to promote the formation of uniform dielectric layers. Wang et al. exploited this method with 3,4,9,10-perylenetetracarboxylic acid (PTCA), forming a uniform and continuous Al_2O_3 layer with TMA and water vapor at a reactor temperature of 100 °C [204]. Alaboson et al. employed 3,4,9,10-perylenetetracarboxylic dianhydride (PTCDA) with similar surface chemistry for the ALD of Al_2O_3, extending the process to HfO_2 using tetrakis(diethylamido)hafnium (TDEAHf) as the Hf source [205]. The need for

functionalization of graphene has been questioned by several groups who managed to grow continuous films on graphene with a simple ALD process [206, 207]. There are many possible reasons for this, many of which are based on the premise that ALD is not a clean process, reactor pressures are such that physisorbed impurity, and precursor species will be present, especially at the lower temperatures required to prevent damage to the 2D material. In a standard self-limiting ALD process, purges are made sufficiently long to remove physisorbed species, several groups exploited this physisorption of precursor molecules to optimize growth [208–211]. It should however be recognized that this is not true ALD, and an approach based on physisorption, and not chemical bonding, would be very difficult to replicate conformally on complex 3D structures.

Although still a widely explored topic, due the relatively low level of functionality of graphene as a consequence of its metallic or semimetallic behavior [212], metal-oxide growth on 2D materials was extended to transition metal dichalcogenides (TMDs). This group of 2D materials was found to exhibit a wide range of electrical properties with band gaps that were tunable with thickness [213]. Akin to graphene, initial studies of the vapor phase growth of oxides on TMDs employed exfoliated flakes to elucidate the physics of material growth and demonstrate device performance. Several TMDs have been investigated – WS_2, $MoSe_2$,WSe_2, and WTe_2 – however, the most widely studied material of this class is MoS_2. Early work on MoS_2 demonstrated that physisorption could be exploited at low temperatures, to give uniform Al_2O_3 thin films by ALD with TMA and H_2O [214]. This was extended to HfO_2, although uniformity was again claimed [215, 216], and it was later demonstrated to be due to the adhesion of impurities promoting HfO_2 growth. It was concluded that HfO_2 growth, directly on the TMDs, was not uniform without pretreatment, even at low temperature [217]. Further studies, with ozone pretreatments enabled uniform ALD growth of both Al_2O_3 and HfO_2 even at higher temperatures, through the formation of Mo—O bonds, an important development for device fabrication [218, 219]. The application of pretreatments to the growth of oxides on other TMDs was successfully employed for both the selenides [220] and tellurides [221]. The shift away from exfoliated flakes to directly grown TMDs further highlights the difficulties in developing schemes to enable metal-oxide growth on 2D materials. CVD grown TMDs are currently relatively poor in quality, as compared with exfoliated materials, particularly those grown at temperatures compatible with CMOS integration [222–224]. Therefore, uniform growth of oxides on the CVD-grown materials maybe misleading and, as the quality of TMD deposition improves, pretreatments and functionalization are likely to be necessary.

1.5 Conclusions

In this review we have introduced the concept of vapor phase growth of metal oxides. Focusing on two case studies, amorphous insulating materials, and ferroelectric oxides, we have illustrated how the nanoscale integration of these metal oxides in electronics has progressed and how the flexibility of the CVD technique

has enabled the growth of highly conformal materials, at the nanometer scale, with precise stoichiometric control to produce complex-layered materials. The ability to produce ultrathin films with composition control in an industry-compatible process cannot be overstated. Although far from exhaustive this snapshot of the drive for integration has shown, the advances are huge, and it has generally been focused on exploiting the bulk properties of the selected materials. However, as scaling approaches the sub-nanometer scale, the prospect of 2D metal oxides, beyond perovskites, maybe realized [225–228]. The quantum confinement effects, due to the inherently low thickness of these materials, open them to a wide range of applications where tunable band structures can enable a range of electrical and optical properties. To date, there has been little progress in vapor phase growth of these layered materials in the 2D domain, primarily as top-down approaches, such as exfoliation from bulk, are sufficient for proof of concept and fundamental materials studies. However, as atomic scale processing methodologies improve, both in terms of addition by growth and removal by etching, the tuning of material phases and interfacial properties that enable the controlled deposition and stabilization of true 2D materials is becoming more widespread; consequently, this is an area where significant materials advances could be made to maintain metal oxides at the forefront of next-generation electronic device materials.

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